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Active stabilisation design of DC–DC converters with constant power load using a sampled discrete-time model: stability analysis and experimental verification

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Abstract: Instabilities of cascade converters with an LC filter in between in power electronic systems have been known, and many answers have been proposed. The load converters are tightly regulated, acting as constant power loads (CPLs). Average models are generally utilised to study the behavior of the converters. For embedded applications, the weight and the volume should be reduced. Consequently, in this case, the limitations of the average method are reached when the cut-off frequency of the LC input filter is close to the switching frequency. Then, other tools are necessary to study this type of system. To overcome this problem, a discrete-time model was developed to study the behavior of the system, taking into account the switching effect. The aim was to enlarge the power range of the stability zone for a DC system composed of a DC–DC boost converter as a source converter, which was connected to the power load via an LC input filter. For this purpose, a stabilisation expression is integrated in the command of the source converter. The stability analysis by the eigenvalues of the system is described using the proposed model. Simulation and experimental results are discussed to verify the proposed stabiliser in different cases.

1 Introduction

Constant power loads (CPLs) are destabilising in nature due to the negative incremental input impedance behaviour. To limit the harmonic effects and electromagnetic interferences, an input load converter (LC) filter is added to the point of load. The stability of CPL depends on the input filter. Negative incremental impedance properties have been commonly studied and are recognised to create instabilities [1–5].

To aid the stabilisation, passive damping circuits with resistors, inductors, capacitors and a small storage converter could be added [6]. Both of these methods augment weight and volume of the system, which has critical characteristics in embedded power systems (e.g. aircraft, ships, and electric cars). Another solution is to change the command of power electronic devices [7]. This can be used in the source [8] and/or load control characteristics. To guarantee stable operation of the system, load commands may be modified. For instance, it is feasible to reduce one or some load control bandwidths thus they are no longer tightly controlled. This makes easy stabilisation, nevertheless reduces load performance [7]. A different example is to include virtual passive damping circuits or a compensator in the command. In [9], a virtual capacitor was inserted on the load side. In [10], a series-connected virtual impedance was utilised on the source side.

The advancement of efficient digital control enables many new techniques to be used such as model predictive control [11], polynomial control [12], and active damping [13].

To investigate the effectiveness of a command, it is required to have a model for the system [14]. In the literature, the average model is widely used to study the behaviour of the converters. The limitations of this method are reached when the cut-off frequency of the LC input filter is close to the switching frequency. To decrease weight and volume, embedded applications force requirements for small values' passive components. This leads to increasing the cut-off frequency of the filter. In this case, to investigate the stability of the system, the usual averaged model is less precise [15, 16].

The variation of the eigenvalues when bifurcation parameters vary can be investigated to learn which bifurcation occurs. A bifurcation demonstrates a qualitative change in the properties of the system depending on these bifurcation parameters [7]. The bifurcation parameters can include load power [14–16], feedback gain [17, 18], capacitance [18], load resistance [18, 19], inductance [20], parasitic resistance of the inductor, switching frequency [21], gain controller [22, 23], compensating ramp [23–25], series resistance of the capacitor [26], input voltage, current reference, and other factors. In this paper, the load power was considered as the bifurcation parameter. Different types of instabilities would exhibit changes when varying the bifurcation parameter because of their non-linear behaviour. Some types of bifurcations found in power electronic systems are periodic doubling (or flip) [17, 18, 21, 23, 24, 26], Neimark–Sacker (or Hopf) [14–16, 21], and saddle-node (or tangent bifurcation) [21].

Knowing how and when a bifurcation happens seems essential. Therefore, suitable modelling is required. Among different modelling approaches for DC–DC converters, the averaged model [23, 24] and discrete-time model [14, 15, 26–28] are commonly found in the literature.

The stability and robustness properties of the system can be investigated by evaluating its eigenvalues [16, 19, 25–30] at the equilibrium point by using the discrete-time or averaged models. In [31], Xu *et al.* have been proposed a non-linear controller for stabilising DC–DC boost converter feeding CPLs. The stability margin of the system regarding the variation of CPL load of the proposed method has been studied.

In this paper, the stability analysis was performed using the discrete-time modelling presented in [15], bifurcation diagrams, and Floquet multipliers.

The methods to actively stabilise the DC link can be classified into three different types: injecting instability information to an output voltage loop, doing the same to the current loop, or

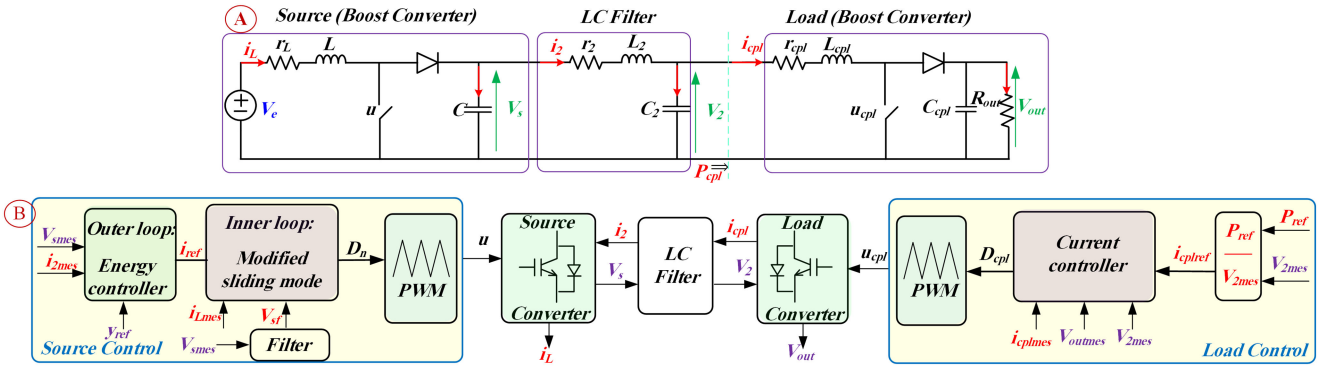


Fig. 1 *System presentation*
(a) Schematic representation of the studied power stage, ***(b)*** Block diagram of the control system

Table 1 System parameters

Parameter	Symbol	Quantity
source converter		
inductive current	i_L	CSV
output voltage	V_s	CSV
duty cycle, command	D_n, u	—
DC input voltage	V_e	63 V
source inductor resistance	r_L	0.4 Ω
source converter inductance	L	2 mH
output capacitance	C	470 μF
switching frequency	F	10 kHz
Load Converter		
inductive current	i_{cpl}	CSV
output voltage	V_{out}	CSV
duty cycle, command	D_{cpl}, u_{cpl}	—
inductor resistance	r_{Lcpl}	0.2 Ω
inductance	L_{cpl}	8.7 mH
capacitance	C_{cpl}	875 μF
resistance	R_{out}	110 Ω
switching frequency	F	10 kHz
LC filter parameters		
inductive current	i_2	CSV
capacitor voltage	V_2	CSV
inductor resistance	r_2	0.12 Ω
inductance	L_2	0.55 mH
capacitance	C_2	38.7 μF (case 1)
capacitance	C_2	60 μF (case 2)
command		
output voltage reference	V_{sref}	100, 150 V
energy controller		
proportional energy term	K_{py}	70
integral energy term	K_{iy}	2500
current controller (source converter)		
current integral term	K_i	1000
current term	λ	1000
current controller (LC)		
current integral term	K_{icpl}	3500
current term	λ_{cpl}	3500
stabiliser		
stabilisation term	K_v	0, 1.2, 0.6
low filter pulsation	w_1	600 rad/s

adjusting the duty cycle directly. This paper focused on the source control modification. The main benefit of modifying the source side exists in the fact that for the load, i.e. the end user, dynamic performance is not modified [32].

In [15], the discrete model for the switching converters including CPL without any stabiliser has been reported. The switching effect is considered. In [7, 32], the discrete model for switching converters with CPL has been presented. The active stabiliser is embedded in the controller of the source converter. We compared the suggested method with the conventional averaging approach and further demonstrated the advantages of our proposed method.

The dynamics of the load by changing the gain of load current controller in the cascaded system was studied [33]. In this paper, we continue to study the same system presented in [15] by adding a stabiliser. The main contributions of this paper include: to extend the stability margin, an active stabiliser is developed. The discrete modelling of this system is developed. The details of modelling are given. The stability analysis of the system is established as an analytical tool to predict the maximum power with changes in the system and control parameters. A map is presented for tuning this stabiliser parameter. Different cases are investigated with the variation of the control parameters and the filter parameter by simulation and experimental results. In addition, the phase portrait for the variation in load power is studied.

This paper is organised as follows: the power stage and command of the studied system are presented in Section 2. It is important that the current controller is based on an adapted indirect sliding-mode controller. The load command is based on only one current controller. Then, the derivation of a discrete-time model is described in Section 3. This model can account for the switching effect. The proposed method can be generalised to multiunit microgrids. This model is achieved with several applications that are explained. The calculation of the Jacobian matrix of the system is summarised. Simulation and experimental results are provided to validate the effectiveness of the proposed stabiliser and its tuning in Sections 4 and 5. The conclusions are presented in Section 6.

2 System presentation

2.1 Power stage

The studied system was composed of a DC–DC boost converter, an LC filter, and a load, as shown in Fig. 1*a* presented in [15]. Both converters operated in continuous current conduction mode with switching period T. The parameters used and the six continuous state variables (CSVs) are shown in Table 1.

The source boost converter is described by the state equations as

$$\begin{cases} \dfrac{\mathrm{d}i_L}{\mathrm{d}t} = \dfrac{1}{L}(V_e - r_L \cdot i_L - (1-u)V_s) \\ \dfrac{\mathrm{d}V_s}{\mathrm{d}t} = \dfrac{1}{C}((1-u)i_L - i_2) \end{cases} \quad (1)$$

The filter can be written by

$$\begin{cases} \dfrac{\mathrm{d}i_2}{\mathrm{d}t} = \dfrac{1}{L_2}(V_\mathrm{s} - V_2 - r_2\, i_2) \\ \dfrac{\mathrm{d}V_2}{\mathrm{d}t} = \dfrac{1}{C_2}(i_2 - i_\mathrm{cpl}) \end{cases} \tag{2}$$

The LC model can be expressed as

$$\begin{cases} \dfrac{\mathrm{d}i_\mathrm{cpl}}{\mathrm{d}t} = \dfrac{1}{L_\mathrm{cpl}}\left(V_2 - r_\mathrm{Lcpl} \cdot i_\mathrm{cpl} - (1 - u_\mathrm{cpl})V_\mathrm{out}\right) \\ \dfrac{\mathrm{d}V_\mathrm{out}}{\mathrm{d}t} = \dfrac{1}{C_\mathrm{cpl}}\left((1 - u_\mathrm{cpl})i_\mathrm{cpl} - \dfrac{V_\mathrm{out}}{R_\mathrm{out}}\right) \end{cases} \tag{3}$$

2.2 Control system

The control of the considered system was realised digitally. At the beginning of each period, the source control variables i_L, i_2, and V_s, and the load control variables i_cpl, V_2, and V_out are sampled one time for each switching period (T). Therefore, six measured variables can be obtained: i_Lmes, i_2mes, V_smes, i_cplmes, V_2mes, and V_outmes. Derivatives and integrators are discretised by a sample time of T. In z-transform, it would be $(1 - z^{-1})/T$ for derivation and $T/(1 - z^{-1})$ for integration, corresponding to a backward Euler as described later in this paper. The integrative term of the error on a variable x is defined by $\mathrm{int}x = \int (x - x_\mathrm{ref})\,\mathrm{d}t$. Both converters are controlled using the structure detailed in Fig. 1*b*. The source control is based on two loops: outer and inner loops. The outer loop controls the energy in the capacitor C. The inner loop controls the current i_L. Only one current loop is considered to control the load current [15].

2.2.1 Energy controller (outer loop): This controller controls the output voltage through the electrostatic energy stored in the output capacitor. y and y_ref are defined as $y = 0.5\mathrm{C}V_\mathrm{smes}^2$ and $y_\mathrm{ref} = 0.5\mathrm{C}V_\mathrm{sref}^2$. By considering the variation of the stored energy as the input power minus the Joule losses and the output power $(\dot{y} = V_\mathrm{e}\, i_\mathrm{ref} - r_\mathrm{L}\, i_\mathrm{ref}^2 - i_\mathrm{2mes}\, V_\mathrm{smes})$, and then combining this equation with a second-order controller $[\dot{y} - \dot{y}_\mathrm{ref} + K_\mathrm{py}(y - y_\mathrm{ref}) + K_\mathrm{iy}\,\mathrm{int}\, y = 0]$ supposing a constant reference ($\dot{y}_\mathrm{ref} = 0$) yields

$$i_\mathrm{ref} = \frac{2P_\mathrm{max}}{V_\mathrm{e}}\left[1 - \sqrt{1 - \frac{V_\mathrm{smes}\, i_\mathrm{2mes} - K_\mathrm{py}(y - y_\mathrm{ref}) - K_\mathrm{iy}\,\mathrm{int}\, y}{P_\mathrm{max}}}\right] \tag{4}$$

where $P_\mathrm{max} = V_\mathrm{e}^2/(4\, r_\mathrm{L})$ and $\mathrm{int}\, y$ are the discrete-time integrator of $y - y_\mathrm{ref}$. The current controller can then calculate the duty cycle of the converter using the current reference i_ref as shown in Fig. 1*b* [15].

2.2.2 Modified sliding-mode controller (inner loop): The inner loop uses an indirect approach sliding-mode controller [34–36]. To augment the stability region of the system, this controller compared with the load controller is adapted via the surface S

$$S = i_\mathrm{Lmes} - i_\mathrm{ref} + K_\mathrm{i}\,\mathrm{int}\, i + K_v\,(V_\mathrm{s} - V_\mathrm{sf}) \tag{5}$$

where $\mathrm{int}\, i$ is the discrete-time integrator of $i_\mathrm{Lmes} - i_\mathrm{ref}$.

K_v is a gain. Its design will be realised, thanks to eigenvalues analysis of the Jacobian matrix obtained in Section 3.2. This will be done for different operating points.

V_sf is the output of a low-pass filter defined by

$$\dot{V}_\mathrm{sf} = \omega_\mathrm{l}(V_\mathrm{smes} - V_\mathrm{sf}) \tag{6}$$

ω_l is the low-pass pulsation. Its value has to be designed widely lower than the cut-off frequency of the LC filter.

Equation (7) is imposed on the derivative of S

$$\dot{S} = -\lambda S \tag{7}$$

Using (1), (4)–(7), the duty cycle D_n is calculated as

$$D_n = \frac{K_v \cdot a_0 + a_1 + a_2}{V_\mathrm{s} - L \cdot i_\mathrm{L} \cdot K_V/C} \tag{8}$$

where

$$\begin{aligned} a_0 &= L\left(\frac{i_\mathrm{2mes} - i_\mathrm{Lmes}}{C} - (\lambda - w_\mathrm{l}) \cdot (V_\mathrm{s} - V_\mathrm{sf})\right) \\ a_1 &= (i_\mathrm{Lmes} \cdot r_\mathrm{L} - V_\mathrm{e} + V_\mathrm{smes}) \\ a_2 &= L((K_\mathrm{i} + \lambda) \cdot (i_\mathrm{ref} - i_\mathrm{Lmes}) - K_\mathrm{i}\,\lambda\,\mathrm{int}\, i) \end{aligned}$$

The voltage controller bandwidth is supposedly smaller than the current controller bandwidth.

2.2.3 Load current controller: The duty cycle of the load controller is given as

$$D_\mathrm{cpl} = \frac{b_\mathrm{l} + b_2}{V_\mathrm{outmes}} \tag{9}$$

where

$$\begin{aligned} b_\mathrm{l} &= i_\mathrm{cplmes}\, r_\mathrm{cpL} - V_\mathrm{2mes} + V_\mathrm{outmes} \\ b_2 &= L_\mathrm{cpl}\left((K_\mathrm{icpl} + \lambda_\mathrm{cpl})(i_\mathrm{cplref} - i_\mathrm{cplmes}) - K_\mathrm{icpl}\,\lambda_\mathrm{cpl}\,\mathrm{int}\, i_\mathrm{cpl}\right) \end{aligned}$$

The commands of both switches u and u_cpl are then generated with a symmetric pulse-width modulation (PWM) [15].

3 Proposed modelling

To realise a model that can be utilised in all frequency ranges, a discrete-time model that includes a switching effect is used. Stability analysis can be made by determining the Jacobian matrix eigenvalues, which provides the values of variables calculated at instants $(n + 1)T$ as a function of variables at instants nT. To find this Jacobian matrix, a model is needed.

3.1 Discrete-time model

A sampled model is presented, for which both duty cycles D_n and D_cpl are constant during each switching period [15].

3.1.1 Definitions: Three vectors of variables are introduced here: $\boldsymbol{X}_\mathrm{c}$, $\boldsymbol{X}_\mathrm{d}$, and $\boldsymbol{X}_\mathrm{mes}$. $\boldsymbol{X}_\mathrm{c}$ and $\boldsymbol{X}_\mathrm{mes}$ represent the six CSV and the six measured values of these variables (Fig. 2*a*)

$$\begin{aligned} \boldsymbol{X}_\mathrm{c} &= \Big[\, i_\mathrm{L} \quad V_\mathrm{s} \quad \underbrace{i_2 \quad V_2}_{\boldsymbol{X}_\mathrm{mes_T}} \quad i_\mathrm{cpl} \quad V_\mathrm{out} \,\Big]^\mathrm{T} \\ &= \Big[\, \underbrace{i_\mathrm{Lmes} \quad V_\mathrm{smes}}_{\boldsymbol{X}_\mathrm{mes}} \quad \underbrace{i_\mathrm{2mes} \quad V_\mathrm{2mes} \quad i_\mathrm{cplmes} \quad V_\mathrm{outmes}}_{\boldsymbol{X}_\mathrm{cplmes}} \,\Big]^\mathrm{T} \end{aligned} \tag{10}$$

$\boldsymbol{X}_{\mathrm{d_T}}$ represents the four discrete variables for the controllers with a supplementary term due to the stabiliser term

$$\boldsymbol{X}_{\mathrm{d_T}} = \Big[\, \mathrm{int}\, i \quad \mathrm{int}\, y \quad \underbrace{\mathrm{int}\, i_\mathrm{cpl}}_{\boldsymbol{X}_\mathrm{dcpl}} \quad V_\mathrm{sf} \,\Big]^\mathrm{T} \tag{11}$$

Equations (1)–(3) are regrouped and put in the following form:

$$\frac{\mathrm{d}X_\mathrm{c}}{\mathrm{d}t} = A_\mathrm{c}\, X_\mathrm{c} + B_\mathrm{c}(X_\mathrm{c})\, U \tag{12}$$

The derivative of X_d can be obtained using (6) and (11). It can be defined as

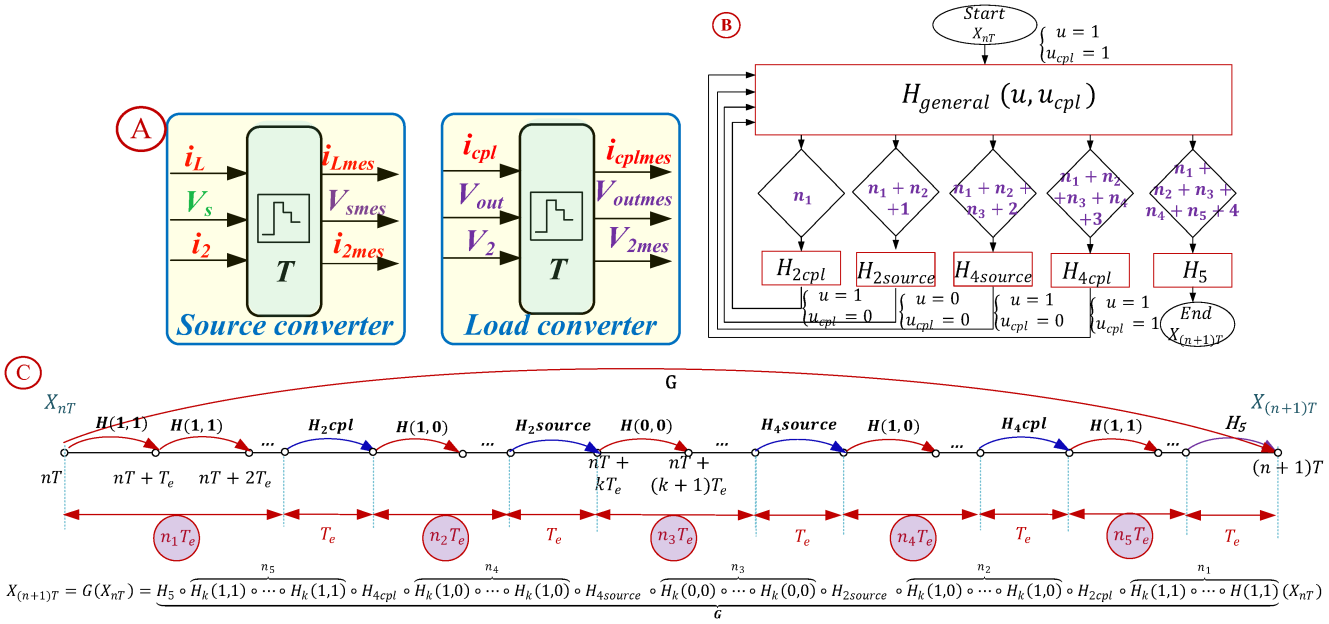


Fig. 2 *Definitions*

(a) CSV and the measured values of these variables, ***(b)*** Flowchart of the discretisation of the maps in each switching period, ***(c)*** Different variables used for discretisation in each switching period

$$\frac{X_{d_{T(n+1)}} - X_{d_{T(n)}}}{T} = \begin{bmatrix} i_{Lmes} - i_{ref} \\ 0.5\ C\left(-V_{sref}^2 + V_{smes}^2\right) \\ i_{cplmes} - \dfrac{P_{ref}}{V_{outmes}} \\ \omega_1(V_{smes} - V_{sf}) \end{bmatrix} \tag{13}$$

$$= A_d \cdot X_{d_{T(n)}} + M_d + N_d\left(X_{d_{T(n)}}\right) + E_n X_{mes_{T(n)}}$$

where

$$A_d = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\omega_1 \end{pmatrix} \quad E_n = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & \omega_1 & 0 & 0 & 0 & 0 \end{pmatrix}$$

$$M_d = \begin{pmatrix} 0 & -0.5\ CV_{sref}^2 & 0 & 0 \end{pmatrix}^t$$

$$N_d = \begin{pmatrix} -i_{ref} & 0.5\ CV_{smes}^2 & -P_{ref}/V_{outmes} & 0 \end{pmatrix}^t$$

3.1.2 Discretisation and recapitulative: The period T is discretised in N_p small steps. T_e is the discretisation period ($T_e = T/N_p$). There are two cases: one where $D_n > D_{cpl}$ and the other where $D_n < D_{cpl}$. The first case is presented; the second one is obtained by the same method. According to Figs. 2*b* and *c*, n_1 is computed as the integer part of $(D_{cpl}T/2)/T_e$. n_2 is the integer part of $((D_nT/2) - (n_1 + 1)T_e)/T_e$. n_3 is the integer part of $((1 - (D_n/2))T - (n_1 + 1 + n_2 + 1)T_e)/T_e$. One can define $n_4 = n_2$ and $n_5 = n_1 - 1$ because of symmetric PWM. Since the carriers are synchronised, it is possible to know the order and length of the switching sequence by comparing the duty cycles.

The applications are summarised here.

In Figs. 2*b* and *c*, $H(1, 1)$, $H(1, 0)$, and $H(0, 0)$ are the general applications and are called for $H(u, u_{cpl})$. These applications are used when both u and u_{cpl} are constant during one discretisation period T_e. The applications $H(u, u_{cpl})$ are calculated utilising the Euler approximation with a step T_e

$$H(u, u_{cpl}): \underbrace{\begin{bmatrix} X_{c\,kTe} \\ X_{d\,(n)T} \\ X_{mes(n)T} \\ X_{dcpl(n)T} \\ X_{cplmes(n)T} \end{bmatrix}}_{X_k} \begin{matrix} u,\ u_{cpl} \\ \text{constant} \\ \rightarrow \end{matrix} \underbrace{\begin{bmatrix} X_{c(k+1)Te} \\ X_{d(n)T} \\ X_{mes(n)T} \\ X_{dcpl(n)T} \\ X_{cplmes(n)T} \end{bmatrix}}_{X_{k+1}}$$

For the applications $H_{2source}$ and $H_{4source}$, the changes of u from 1 to 0 and from 0 to 1 have to be taken into account

$$H_{2source}: \underbrace{\begin{bmatrix} X_{c\,kTe} \\ X_{d\,(n)T} \\ X_{mes(n)T} \\ X_{dcpl(n)T} \\ X_{cplmes(n)T} \end{bmatrix}}_{X_k} \begin{matrix} u = 1 \\ \rightarrow \\ u_{cpl} \\ \text{cst} \end{matrix} \underbrace{\begin{bmatrix} X_{c(k+d_k)Te} \\ X_{d(n)T} \\ X_{mes(n)T} \\ X_{dcpl(n)T} \\ X_{cplmes(n)T} \end{bmatrix}}_{X_{k+d_k}} \begin{matrix} u = 0 \\ \rightarrow \\ u_{cpl} \\ \text{cst} \end{matrix} \underbrace{\begin{bmatrix} X_{c(k+1)Te} \\ X_{d(n)T} \\ X_{mes(n)T} \\ X_{dcpl(n)T} \\ X_{cplmes(n)T} \end{bmatrix}}_{X_{k+1}}$$

$$k = \begin{cases} n_1 + n_2 + 1 & D > Dcpl \\ n_1 & D < Dcpl \end{cases}$$

$$H_{2cpl}: \underbrace{\begin{bmatrix} X_{c\,kTe} \\ X_{d\,(n)T} \\ X_{mes(n)T} \\ X_{dcpl(n)T} \\ X_{cplmes(n)T} \end{bmatrix}}_{X_k} \begin{matrix} u_{cpl} = 1 \\ \rightarrow \\ u \\ \text{cst} \end{matrix} \underbrace{\begin{bmatrix} X_{c(k+d_k)Te} \\ X_{d(n)T} \\ X_{mes(n)T} \\ X_{dcpl(n)T} \\ X_{cplmes(n)T} \end{bmatrix}}_{X_{k+d_k}} \begin{matrix} u_{cpl} = 0 \\ \rightarrow \\ u \\ \text{cst} \end{matrix} \underbrace{\begin{bmatrix} X_{c(k+1)Te} \\ X_{d(n)T} \\ X_{mes(n)T} \\ X_{dcpl(n)T} \\ X_{cplmes(n)T} \end{bmatrix}}_{X_{k+1}}$$

$$k = \begin{cases} n_1 & D > Dcpl \\ n_1 + n_2 + 1 & D < Dcpl \end{cases}$$

H_{2cpl} and H_{4cpl} can be calculated in the same manner

$$H_{4\text{source}}:\begin{bmatrix}\boldsymbol{X}_{\text{c}\,kT\text{e}}\\ \boldsymbol{X}_{\text{d}\,(n)\text{T}}\\ \boldsymbol{X}_{\text{mes}(n)\text{T}}\\ X_{\text{dcpl}(n)\text{T}}\\ \underbrace{X_{\text{cplmes}(n)\text{T}}}_{X_k}\end{bmatrix}\begin{matrix}u=0\\ \rightarrow\\ u_{\text{cpl}}\\ \text{cst}\end{matrix}\begin{bmatrix}\boldsymbol{X}_{\text{c}(k+\text{d}_k)T\text{e}}\\ \boldsymbol{X}_{\text{d}(n)\text{T}}\\ \boldsymbol{X}_{\text{mes}(n)\text{T}}\\ X_{\text{dcpl}(n)\text{T}}\\ \underbrace{X_{\text{cplmes}(n)\text{T}}}_{X_{k+\text{d}_k}}\end{bmatrix}\begin{matrix}u=1\\ \rightarrow\\ u_{\text{cpl}}\\ \text{cst}\end{matrix}\begin{bmatrix}\boldsymbol{X}_{\text{c}(k+1)T\text{e}}\\ \boldsymbol{X}_{\text{d}(n)\text{T}}\\ \boldsymbol{X}_{\text{mes}(n)\text{T}}\\ X_{\text{dcpl}(n)\text{T}}\\ \underbrace{X_{\text{cplmes}(n)\text{T}}}_{X_{k+1}}\end{bmatrix}$$

$$k=\begin{cases}n_1+n_2+n_3+2 & D>D\text{cpl}\\ n_1+n_2+n_3+n_4+3 & D<D\text{cpl}\end{cases}$$

$$H_{4\text{cpl}}:\begin{bmatrix}\boldsymbol{X}_{\text{c}\,kT\text{e}}\\ \boldsymbol{X}_{\text{d}\,(n)\text{T}}\\ \boldsymbol{X}_{\text{mes}(n)\text{T}}\\ X_{\text{dcpl}(n)\text{T}}\\ \underbrace{X_{\text{cplmes}(n)\text{T}}}_{X_k}\end{bmatrix}\begin{matrix}u_{\text{cpl}}=0\\ \rightarrow\\ u\\ \text{cst}\end{matrix}\begin{bmatrix}\boldsymbol{X}_{\text{c}(k+\text{d}_k)T\text{e}}\\ \boldsymbol{X}_{\text{d}(n)\text{T}}\\ \boldsymbol{X}_{\text{mes}(n)\text{T}}\\ X_{\text{dcpl}(n)\text{T}}\\ \underbrace{X_{\text{cplmes}(n)\text{T}}}_{X_{k+\text{d}_k}}\end{bmatrix}\begin{matrix}u_{\text{cpl}}=1\\ \rightarrow\\ u\\ \text{cst}\end{matrix}\begin{bmatrix}\boldsymbol{X}_{\text{c}(k+1)T\text{e}}\\ \boldsymbol{X}_{\text{d}(n)\text{T}}\\ \boldsymbol{X}_{\text{mes}(n)\text{T}}\\ X_{\text{dcpl}(n)\text{T}}\\ \underbrace{X_{\text{cplmes}(n)\text{T}}}_{X_{k+1}}\end{bmatrix}$$

$$k=\begin{cases}n_1+n_2+n_3+n_4+3 & D>D\text{cpl}\\ n_1+n_2+n_3+2 & D<D\text{cpl}\end{cases}$$

The last application H_5 allows the updating of the variables at instants $(n+1)T$

$$H_5:\begin{bmatrix}\boldsymbol{X}_{\text{c}\,kT\text{e}}\\ \boldsymbol{X}_{\text{d}\,(n)\text{T}}\\ \boldsymbol{X}_{\text{mes}(n)\text{T}}\\ X_{\text{dcpl}(n)\text{T}}\\ \underbrace{X_{\text{cplmes}(n)\text{T}}}_{X_k}\end{bmatrix}\begin{matrix}u=1\\ \rightarrow\\ u_{\text{cpl}}=1\end{matrix}\begin{bmatrix}\boldsymbol{X}_{\text{c}(k+1)T\text{e}}\\ \boldsymbol{X}_{\text{d}(n+1)\text{T}}\\ \boldsymbol{X}_{\text{mes}(n+1)\text{T}}\\ X_{\text{dcpl}(n+1)\text{T}}\\ \underbrace{X_{\text{cplmes}(n+1)\text{T}}}_{X_{n+1}}\end{bmatrix}$$

The application G is presented in Fig. 2*c*, where $\boldsymbol{H}_k(u,\,u_{\text{cpl}})$ is the application $H(u,\,u_{\text{cpl}})$ calculated at an instant $nT+kT_{\text{e}}$.

Remark: Owing to the symmetric and synchronised PWM, we know the switching sequence will generally be 11 01 00 10 11 or 11 10 00 01 11. There is one particular case (when both duty cycles are equal or very close), where the switching sequence is 11 00 11. This particular case needs a special transition function that is obtained in the same way as the ones presented in this paper ($H_{2\text{cpl}}$, $H_{2\text{source}}$, $H_{4\text{cpl}}$, and $H_{4\text{source}}$). The algorithm chooses at each instant the correct function to use, depending on the state of the converter.

3.2 Jacobian matrix

$\boldsymbol{H}_k$ are vector functions $\boldsymbol{H}_k$: $\mathbb{R}^{16}\rightarrow\mathbb{R}^{16}$ transforming X_k into $X_{k+1}=\boldsymbol{H}_k(X_k)$. In a matrix representation, it would be a square matrix of size 16. These $\boldsymbol{H}_k$ matrices are not explicitly expressed, the Jacobian $\boldsymbol{J}_{H_k}$ is directly calculated as

$$\boldsymbol{J}_{H_k}=\begin{bmatrix}\dfrac{\partial X_{k+1}[1]}{\partial X_k[1]} & \cdots & \dfrac{\partial X_{k+1}[1]}{\partial X_k[16]}\\ \vdots & \ddots & \vdots\\ \dfrac{\partial X_{k+1}[16]}{\partial X_k[1]} & \cdots & \dfrac{\partial X_{k+1}[16]}{\partial X_k[16]}\end{bmatrix}$$

The Jacobian matrix of G, denoted as $\boldsymbol{J}_G$, can be calculated by multiplying the Jacobian matrices of each $\boldsymbol{H}_k$. Therefore, its eigenvalues can be calculated in order to investigate the system stability. If eigenvalues are in the unit circle, the system is stable; if they are exterior, the system becomes unstable [11].

4 Simulation results

Since the command is realised digitally, a time delay should be considered. This delay is due to the time required to sample, calculate, and update the duty cycle. As a result, the duty cycles D_n (8) and D_{cpl} (9) applied in one switching period depend on the situation at the commencement of the earlier period. To validate the proposed model, simulation results are presented, taking into account the delay. The parameters are detailed in Table 1.

To validate the model, MATLAB/Simulink was used:

- Section 4.1: time-domain waveforms are given.
- Section 4.2: the evolution of eigenvalues for the load power variation is shown with and without the stabiliser using the proposed model.
- Section 4.3: phase plans for the two cases with and without stabiliser are shown.
- Section 4.4: robustness properties with and without the stabiliser.

4.1 Time domain

The current controller parameters of the source and LCs are set as $K_i=\lambda=1000$ and $K_{\text{icpl}}=\lambda_{\text{cpl}}=3500$, respectively. In Fig. 3*a*, the waveforms of the inductive current for the source boost converter (i_{L}), the LC filter (i_2), and the LC (i_{cpl}) are shown with the stabiliser gain $K_v=0$. The reference power (P_{ref}) changes stepwise from 400 to 650 W. One has a small power load. In this case, the system is stable. In another case, the power load is higher. In this case, oscillations occur in which the system is unstable.

4.2 Eigenvalues

The eigenvalues from the matrix $\boldsymbol{J}_G$ allow investigation of the asymptotic stability of the system around the equilibrium point. The evolution of Floquet multipliers is presented for two cases, without and with the stabiliser.

4.2.1 Without stabiliser: In Fig. 3*b*, discrete-time eigenvalues are presented with applying step changes in the load power reference 400 W → 650 W. The eigenvalue corresponding to the time component was removed because it was always equal to 1. The modulus of the eigenvalues shown in Fig. 3(B2) indicates that the critical power is approximately $P_0=600$ W. Below this power, the system is stable. Above this power, the system becomes unstable. As shown in Fig. 3(B1), the eigenvalues that leave the unit circle are a pair of complex conjugates. In another word, the system with a Neimark–Sacker bifurcation [11, 23] loses its stability. It is the equivalent to Hopf bifurcation, but for discrete systems.

In Fig. 3*c*, the bifurcation diagram of the input inductor current i_{L} is presented, considering the power as the bifurcation parameter. The bifurcation occurs when the load power is P_0. The maximum stable power, obtained from the eigenvalues, is consistent with the bifurcation point presented from the bifurcation diagram.

4.2.2 With stabiliser: Stable and unstable operating points can be obtained using the eigenvalues modulus from the matrix $\boldsymbol{J}_G$. Fig. 4*a* shows the unstable and stable operating points for the load power from 400 to 850 W and the stabilisation gain K_v from 0 to 1.6. These results were obtained using the proposed sampled model. This map shows that the maximum power is increased when the stabiliser parameter (K_v) varies. This map facilitates the tuning of the stabiliser parameter.

We set $K_v=1.2$. In Fig. 4*b*, Floquet multipliers corresponding to the proposed model are shown when the load power reference changes from 400 to 850 W.

In Fig. 4*c*, the bifurcation diagram of the input inductor current i_{L} is presented, where the power is regarded as the bifurcation parameter. The bifurcation occurs when the load power is P_0. It shows that the maximum power is increased when the stabiliser is used. This proves the Jacobian matrix calculation. The proposed

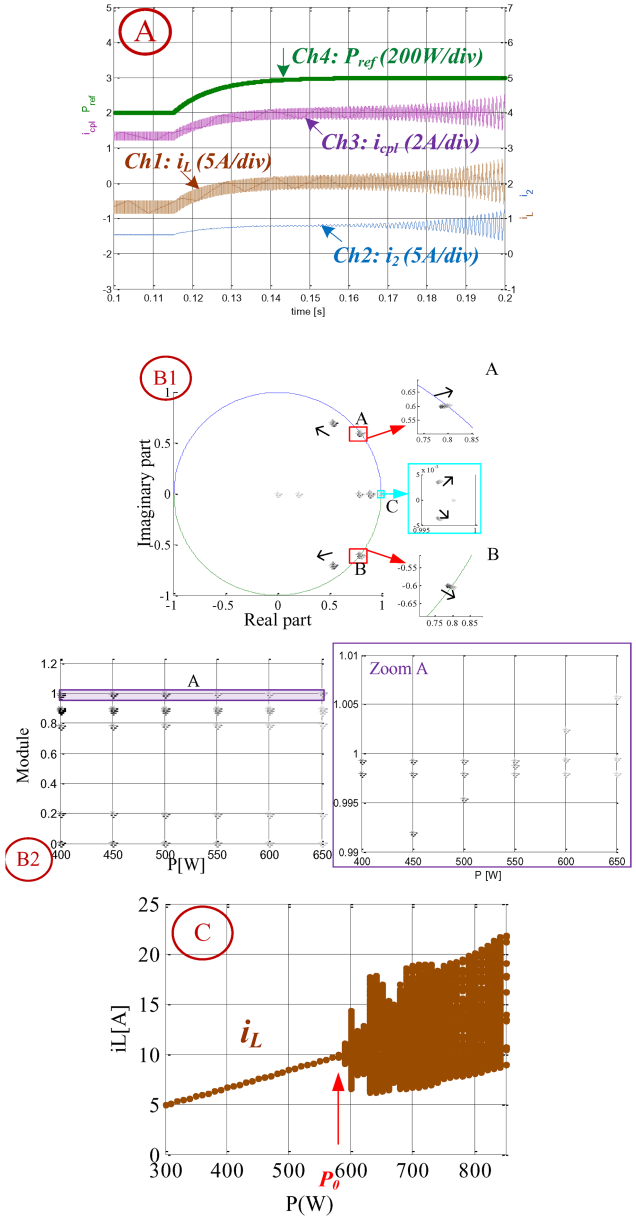


Fig. 3 *Simulation results without stabilizer*

(a) Simulation waveforms without stabilisation, after a power change, stepwise 400→650 W, with $K_V = 0$, $K_i = \lambda = 1000$, $V_{sref} = 150$ V (case 1), ***(B1)*** Evolution of Floquet multipliers for the load power variation from 400 to 650 W; arrows show increasing power, ***(B2)*** Eigenvalues module for the variation of load power from 400 to 650 W and zoom near 1 in view of A (case 1), ***(c)*** Bifurcation diagram representing multiple samples of i_L at each power without stabiliser

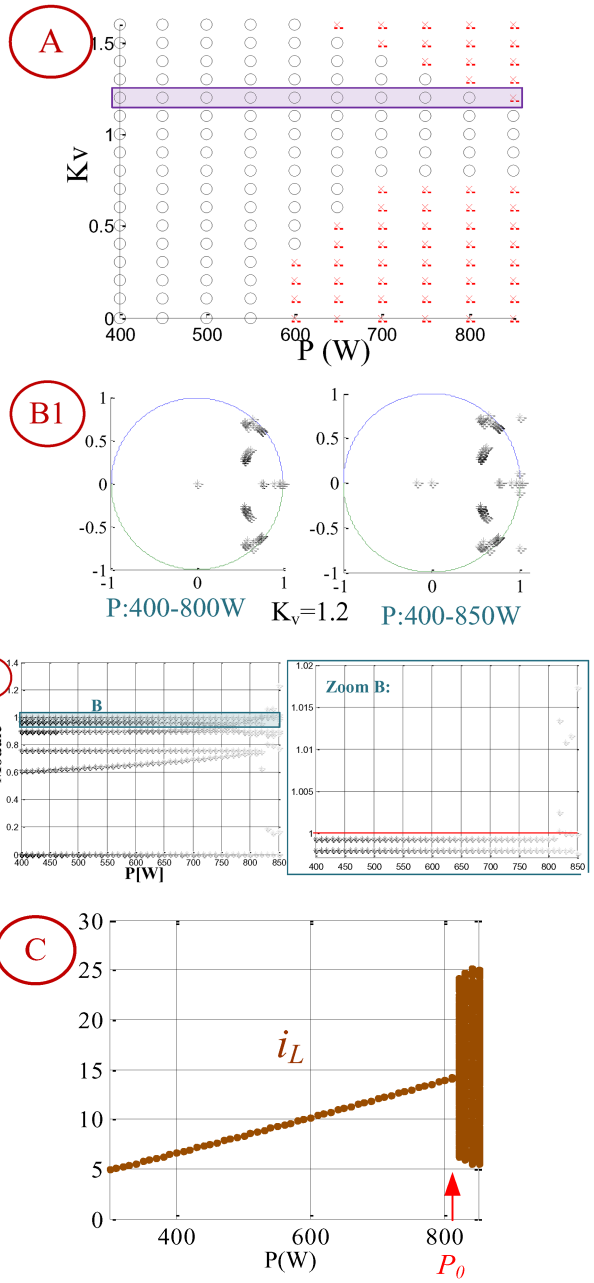


Fig. 4 *Performance of the stabilizer*

(a) Stable and unstable operating points, using the proposed model. Black circles show stable operating points and red crosses specify unstable operating points (case 1), ***(B1)*** Evolution of Floquet multipliers for the load power of the variation. Middle: module of the eigenvalues for the variation of load power from 400 to 850 W, ***(B2)*** Zoomed in view of B (case 1), ***(c)*** Bifurcation diagram representing multiple samples of i_L at each power level with stabiliser

model can accurately predict the boundary where the system is stable.

Fig. 5*a* illustrates the stable and unstable operating points for the load power variation from 300 to 850 W and the stabilisation gain K_v from 0 to 1 for case 2.

Finally, in Fig. 5*b*, the response to a step current is compared with and without stabiliser to see the dynamic effect at the beginning of a step. Although the oscillations are somewhat larger immediately after the step, they become lower in ∼100 ms. The maximum current is ∼2 A more (19 A with stabiliser and 17 A without), so it is not a significant issue for the current ratings of the components.

4.3 Phase plan

In this section, the phase portrait for the variation of load power for two cases is presented. The gain of the stabiliser is set to $K_v = 0$. Fig. 5*c* (a) represents the response to a filtered power step from 300 to 600 W. The voltage of the filter (V_2) is plotted against the inductive current (i_2) of the LC filter. The gain of the stabiliser is set to $K_v = 1.2$. Fig. 5*c* (*b*) shows the response to the same step, but with a stabilising command. In the first case, the system oscillates after going to the second operating point, up to an ellipse that shows upper limit oscillations. In the second case, the system remains stable at the second operating point.

4.4 Robustness properties

Fig. 4*a* presented the unstable and stable operating points. In this section, the stability margin regarding the variation of the LC input filter is presented.

For robustness analysis, it is possible to investigate the behaviour of the system when other parameters vary. Fig. 6 presents the evolution of eigenvalues when the values of L_2 and C_2 are changed while the filter cut-off frequency $w_2 = 1/\sqrt{(L_2C_2)}$ is

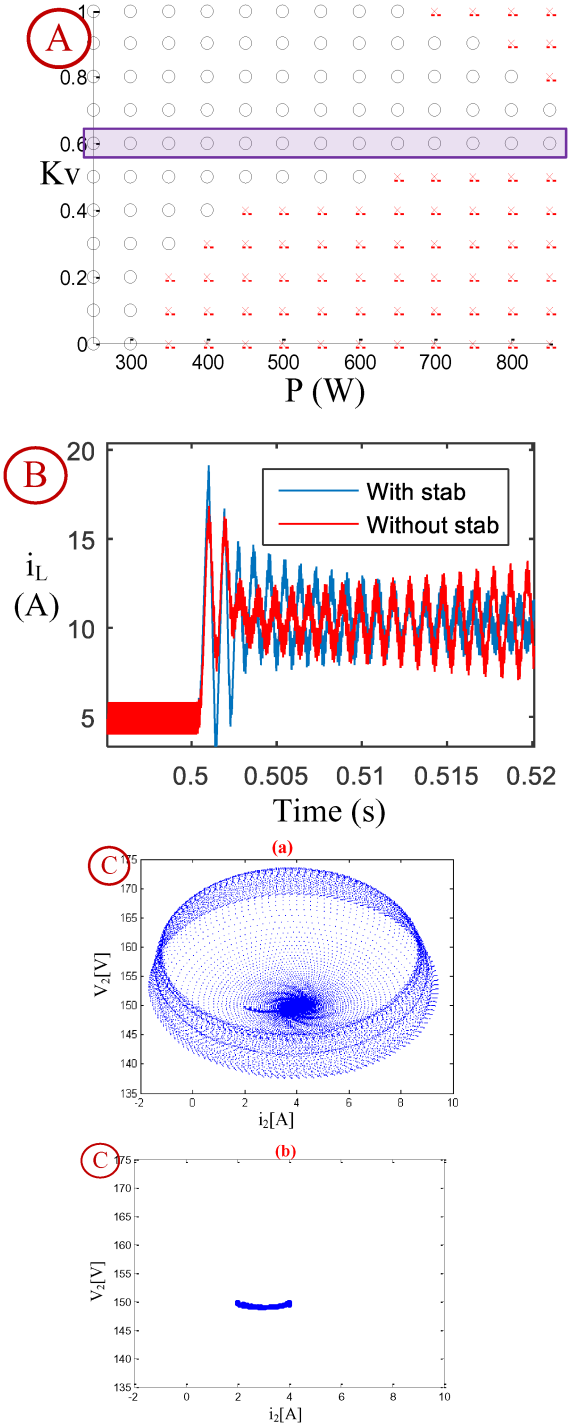


Fig. 5 *With and without the stabilizer*

(a) Stable and unstable operating points using the proposed model. Black circles show stable operating points and red crosses specify unstable operating points (case 2), ***(b)*** Comparison of a current step with and without stabilisations, ***(c)*** Phase portrait for the load power variation from 300 to 600 W, and $K_i = \lambda = 1000$, $V_{sref} = 150$ V (case 1): (a) $K_V = 0$ and (b) $K_V = 1.2$

constant. The value of L_2 varies from 0.35 to 0.7 mH for the power reference varied from 400 to 900 W. This paper is done for the two cases with $K_v = 1.1$ and 1.2 as well as without stabiliser ($K_v = 0$).

This paper shows that the system is stable even if the system parameters change within a large range.

5 Experimental results

As presented in Fig. 7*a*, in order to validate the proposed method, the stability region, and the critical powers, an experimental bench was implemented. The DC input voltage (V_e) was provided by a programmable power supply. The maximum source current is

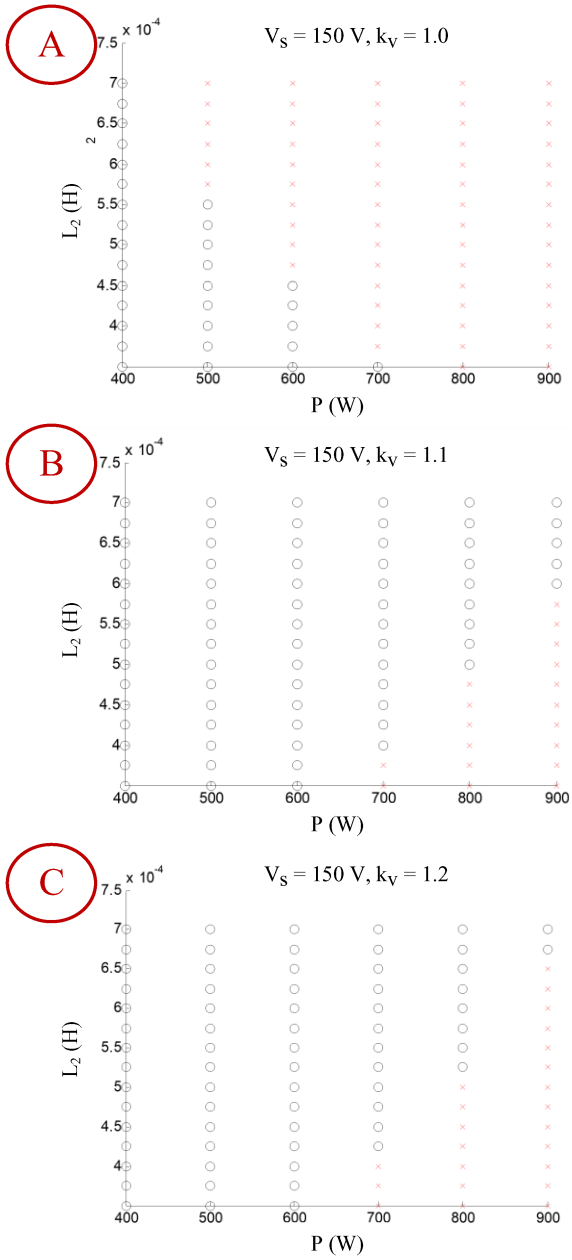


Fig. 6 *Stable and unstable operating points for the variation of L_2 and C_2 when the load power is changed, holding the filter cut-off frequency $w_2 = 1/\sqrt{(L_2C_2)}$ constant, with $V_{sref} = 150$ V (case 1). Black circles show stable operating points and red crosses specify unstable operating points*

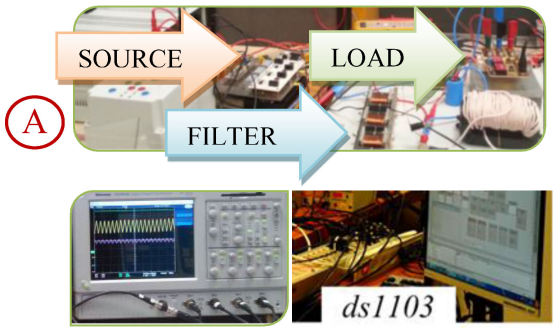
(a) $K_V = 0$, ***(b)*** $K_V = 1.1$, ***(c)*** $K_V = 1.2$

limited to 10 A. A TDK-Lambda 60 V/85 A was used as DC power supply. For the source converter, Semikron trench insulated gate bipolar transistors: SKM50GB123D was used. For LC, was SKM195GB126D. PWM was performed by a dSPACE real-time control card (DS1103). This card was connected to a personal computer with the corresponding MATLAB/Simulink toolbox. Experimental results were provided by Tektronix digital oscilloscopes (TDS5034B). Langlois voltage differential probes model ISOL-710 with a bandwidth of 25 MHz and Chauvin-Arnoux AC/DC current clamps model E3N 10/100 A with a bandwidth of 100 MHz were used to measure the voltages and currents, respectively.

The experimental parameters are given in Table 1. The values of the filter parameters for the two cases are given.

In this section, different cases are described with the variation of the control parameters and the filter parameter.

Four axes were tested corresponding to the different states of the system:



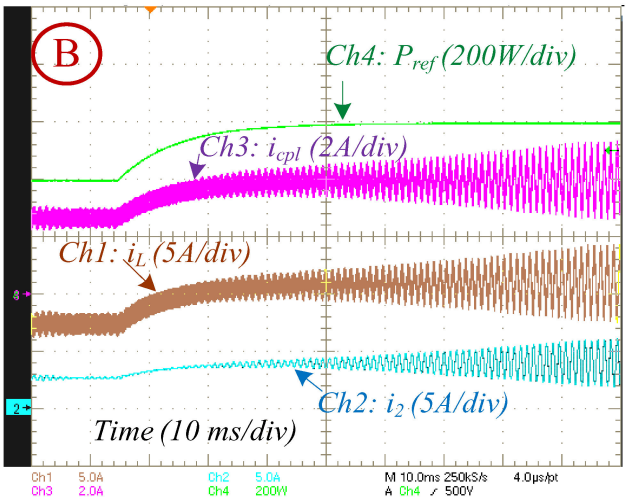


Fig. 7 *Experimental results*

(a) Experimental setup consisting of source and LCs, LC filter, oscilloscope, and dSPACE real-time control card, ***(b)*** Experimental waveforms without stabilisation, after a power change, stepwise 400→650 W, $K_i = \lambda = 1000$, $K_{icpl} = \lambda_{cpl} = 3500$, $V_{sref} = 150$ V, $K_v = 0$ (case 1)

1. Verification of the time-domain waveforms.
2. B1 – performance of the stabiliser.
3. B2 – phase portrait for the variation in load power.
4. B3 – performance of the stabiliser with the variation of the filter parameter (case 2).
5. B4 – performance of the stabiliser with the variation of the reference output voltage.

5.1 Time-domain waveforms

The gain of the stabiliser was put to $K_v = 0$. Fig. 7*b* shows the behaviour of the system when the load power is changed.

The current controller parameters of the source converter were set as $K_i = \lambda = 1000$. The current controller parameters of the LCs were set as $K_{icpl} = \lambda_{cpl} = 3500$.

The experimental waveforms of the currents [(i_L), (i_2), and (i_{cpl})] are shown with the filtered power step (P_{ref}). One is for a small load power (400 W) (a stable operating point); and the other is for a higher load power (650 W), (an unstable operating point). The oscillation is highly significant in the end and begins shortly following the step. Fig. 7*b* validates the results obtained from Fig. 3*a*.

5.2 Performance of the stabiliser

5.2.1 Performance of the stabiliser (case 1): Fig. 8 shows the behaviour of the system while a load power step (P_{ref}) from 300 to 700 W was applied in two cases: Fig. 8*a*, with $K_v = 0$, related to a command with no stabilisation; and Fig. 8*b*, with stabilisation ($K_v = 1.2$). It can be observed that in the next case, oscillations on the inductive current (i_2) of the LC filter, and the inductive current (i_{cpl}) of the LC no longer existed. Therefore, the adapted command gives

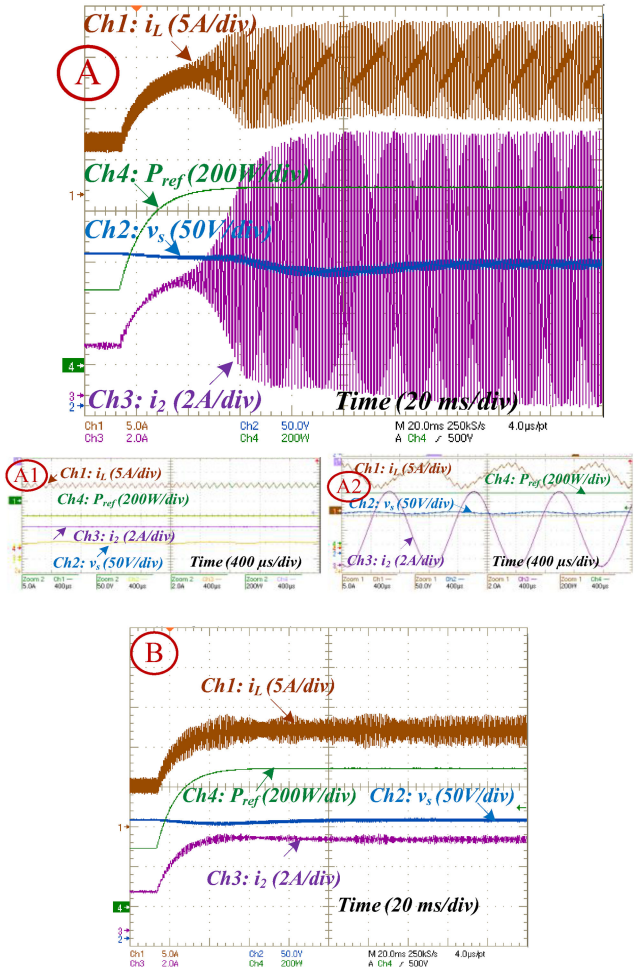


Fig. 8 *Performance of the stabiliser*

(a) Experimental waveforms of currents with a power step from 300 to 700 W, without stabilisation ($K_v = 0$), ***(A1)*** zoom earlier than the step, ***(A2)*** zoom after the step; $K_i = \lambda = 1000$, $K_{icpl} = \lambda_{cpl} = 3500$, $V_{sref} = 150$ V (case 1), ***(b)*** With stabilisation ($K_v = 1.2$)

to the stabilisation of the DC grid side. These results confirm those obtained in Figs. 4*a* and *b*.

5.2.2 Phase portrait for the load power variation: In this section, the response for a filtered power step is compared with and without stabiliser experimentally.

Figs. 9*a* and *b* represent the experimental phase portrait for the load power variation from 300 to 600 W. V_2 and i_2 are viewed in *XY* mode. V_2 is plotted against i_2. To observe the voltage visibly, the AC input coupling of the oscilloscope was used for both cases.

Fig. 9*a* shows the response to the filtered power step when the gain of the stabiliser (K_v) is set to zero.

Fig. 9*b* shows the response to the same step when the gain of the stabiliser is set to $K_v = 1.2$.

In the first case (Fig. 9*a*), as mentioned previously, in Section 4.3, the system began to oscillate after going to the next equilibrium point, up to a circle that shows maximum oscillations. In another word, the system trajectory moves from a stable operating point to unstable limit cycle oscillations.

In the second case (Fig. 9*b*), the system remained stable at the second operating point. This verifies the results obtained from Figs. 5*c* (a) and (b).

5.2.3 Performance of the stabiliser with the variation of the filter parameter: Figs. 10*a* and *b* show the behaviour of the system while a load power step (P_{ref}) from 300 to 600 W was related in two cases: Fig. 10*a*, with $K_v = 0$, subsequent to a command without stabilisation; and Fig. 10*b*, with stabilisation ($K_v = 0.6$). The experimental waveforms of the inductive current (i_L) of

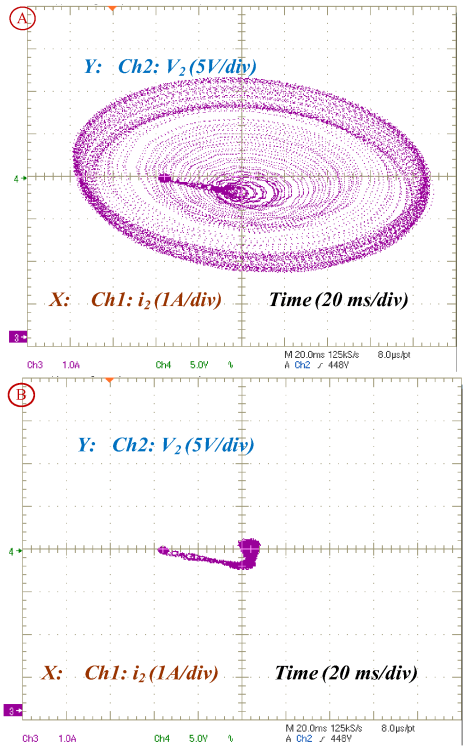


Fig. 9 *Experimental phase portrait after a load power change, stepwise 300→600 W,* $K_i = \lambda = 1000$, $K_{icpl} = \lambda_{cpl} = 3500$, $V_{sref} = 150$ V *(case 1)*
(a) $K_V = 0$, ***(b)*** $K_V = 1.2$

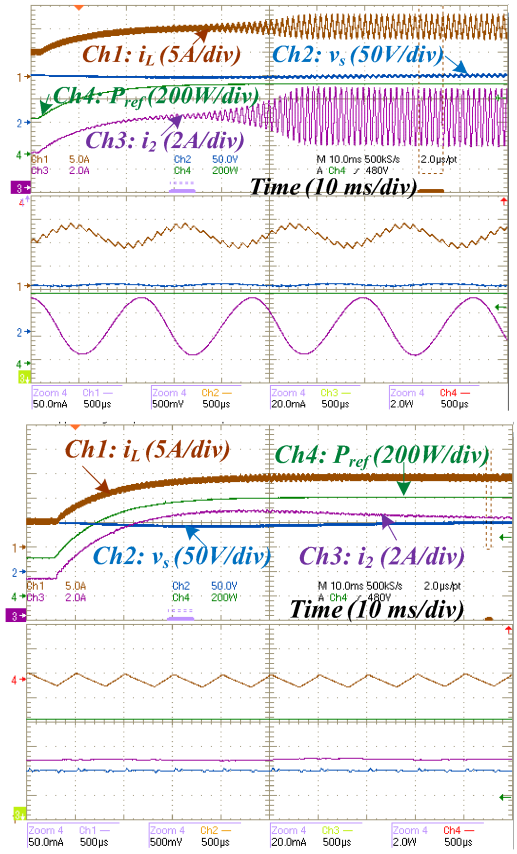


Fig. 10 *Top: experimental waveforms of currents with a filtered power step from 300 to 600 W,* $K_i = \lambda = 1000$, $K_{icpl} = \lambda_{cpl} = 3500$, $V_{sref} = 100$ V*; bottom: zoom after the step (case 2)*
(a) Without stabilisation ($K_V = 0$), ***(b)*** With stabilisation ($K_V = 0.6$)

the source converter, the output voltage (V_s) of the source boost converter, and the inductive current (i_2) of the LC filter are given

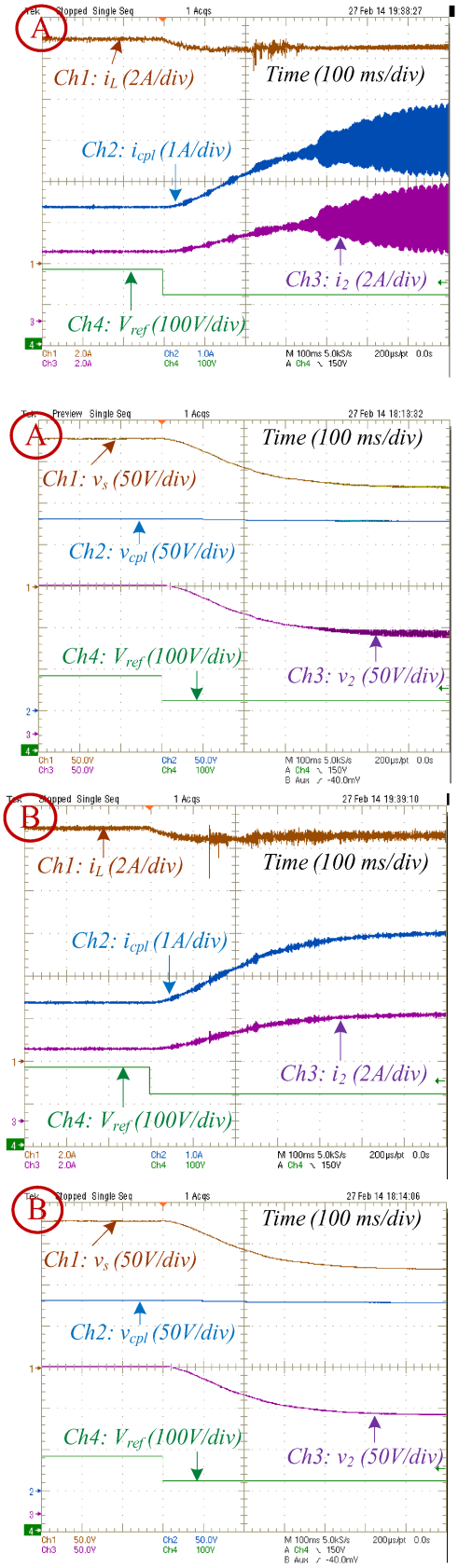


Fig. 11 *Experimental waveforms of a reference voltage step from 180 to 120 V at Pref = 600 W*
(a) Without stabilisation, ***(b)*** With stabilisation

with the filtered power step (P_{ref}). These results confirm the obtained Fig. 5*a*.

Some systems may require a varying bus voltage, so a reference voltage step is shown in Fig. 11. Since the maximum stable power

increases with the bus voltage, it is expected that the system will become unstable when the voltage is reduced. That means the power should be reduced as well without a stabiliser. When it is activated, it is possible to keep the same power while remaining in stable operation.

6 Conclusion

This paper presents an active stabiliser to improve the asymptotic stability of a system collected of a DC–DC boost converter, an LC, and an LC filter in between. The studied system is presented with its associated command. The control uses two loops: an energy controller in the outer loop and a current controller in the inner loop. The current loop is based on an indirect approach sliding-mode controller. Stabilisers found in the literature often modify the reference of the power or of the current. Here, the current loop is modified to directly include the stabilisation. Stability analysis of this system was performed using a discrete-time modelling. The switching effect is taken into account in the proposed model. Thanks to the eigenvalues of the Jacobian matrix, it is possible to study robustness properties with regard to system parameter variations. As an example, a variation in power was investigated. The analysis of stability demonstrates that this control can stabilise the system. The bifurcation diagrams show the maximum power is increased when the stabiliser is used. Therefore, owing to the customised control approach, an improvement of the power range of the stability zone has been realised. The usefulness of the stabiliser and its tuning were validated by simulation and experimental results. In addition, the performance of the stabiliser with the variation of the filter parameter is shown. The simulation results are consistent with the experimental results.

7 Acknowledgment

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