A Current-mode PID Controller Using Voltage Differencing Gain Amplifiers

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***Abstract*—This paper presents an electronically tunable current-mode proportional-integral-derivative (PID) controller based on voltage differencing gain amplifier (VDGA). The circuit structure uses low component count consisting of 2 VDGAs and 2 capacitors, without any resistor, suitable to implement into integrated circuit. This PID controller is independently tunable with electronic method. The simulation results demonstrating the performances of the proposed PID controller are given by PSPICE. Additionally, a closed-loop system as an example is introduced. The closed loop feedback control system of PID controller and low pass filter has total power consumption approximately 5.6mW, at ±1.5V.**

Keywords—VDGA, Current-mode circuit, PID controller, Independent tuning, Low component, Closed-loop system

I. INTRODUCTION

PID controllers are important parts in control engineering works, used in many areas such as signal processing, temperature control, speed motor control and etc. The equation of PID has three terms consisting of P meaning proportional term, I is integral term and D is derivative term. The PID controller has been growing developed based on different active devices [1]-[9]. From our literature review, we found that the PID controllers using current conveyors [1-2], operating transconductance amplifier (OTA) [3], second generation current controlled conveyor (CCCII) [4], second generation current conveyor (CCII) [5], current differencing buffered amplifier (CDBA) [6], differential difference current conveyor (DDCC) [7] employ many active and passive components. The PID controller using current controlled current differential buffer amplifiers (CCCDBAs) [8] use many active devices and have to use current splitter, which make circuit more complicated. The PID controller based on current feedback operational amplifier (CFOA) [9], Z-copy current follower transconductance amplifier (ZC-CFTA) [10] use only single active device and four passive elements. Unfortunately, they cannot be independently tunable. Recently, PID controller use the DDCC [11] was proposed. Even its parameters can be independently tuned, many of passive elements must be implemented.

Voltage differencing buffered amplifier (VDBA) was recently presented in many applications [12-13], it is an interesting active building block, since its can be electronically tuned current gain at port z by adjusting trans-conductance gain through external bias current. However, its voltage gain at w port cannot be adjusted. To extend workability, VDGA was introduced in 2013 [14]. The current gain at z port including the voltage gain at w port of the VDGA can be also electronically tunable via the trans-conductance gain through corresponding bias currents. With the mentioned features, it is very suitable for circuit design via microcontroller-based control for a smart application. The tendency of VDGA usage is being more popular, we have investigated that the VDGA was applied in many circuit applications, for instance, in filter designs [14]-[15] and oscillator [16]. Until now, there is still no its application in controller circuits.

Presently, a current-mode circuit has been increasingly used to developed circuit design more popular than voltage-mode because the need of reducing a supply voltage of electronic apparatus to be a low voltage including low power architecture. Consequently, the current-mode technique is an alternative method appropriate for mentioned requirement. Moreover, the circuits designed with the current-mode technique have more several features. Examples of the mentioned advantages are larger dynamic range, higher bandwidth, lower power consumption, no need summing circuit and linearity and etc [17-21].

The objective of this article is to introduce a novel current-mode PID controller with minimum passive and active elements. Simultaneously, it still offers the advantage of independent/electronic tenability of gain P (K_P), gain I (K_I), and gain D (K_D) parameters via the relative bias currents of the VDGAs employ in the proposed circuit. The circuit structure consisted of only two VDGAs and two capacitors (one for floating capacitor and one for grounded capacitor), without using external resistor. The simulation result was carried out as well to illustrate the performance of the proposed controller, for example the frequency response, independent/electronic tenability and step response. Furthermore, the application and performance of the proposed VDGA-based PID controller in a closed-loop control system are also investigated, according to theory.

II. BASIC OF VDGA

A. The Concept of Voltage Differencing Gain Amplifier

The active building block used in the work is VDGA. We can control output i_z by adjusting bias current I_{BA}, control current gain i_x by adjusting I_{BB} and control voltage gain v_w by adjust ratio of I_{BB} and I_{BC} The symbol, equivalent circuit and CMOS internal construction of the VDGA are shown in Fig. 1. Fig. 2 depicts a CMOS implementation of the VDGA. The characteristic of VDGA is depicted.

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_{mA} & -g_{mA} & 0 & 0 & 0 \\ 0 & 0 & 0 & -g_{mB} & 0 \\ 0 & 0 & 0 & \dfrac{g_{mB}}{g_{mC}} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_x \\ v_z \\ v_w \end{bmatrix}, \qquad (1)$$

where g_{mA}, g_{mB} and g_{mC} are transconductance gain of VDGA with controllable by adjust bias current I_{BA}, I_{BB} and I_{BC}. The relation of each g_m is

$$g_{mk} = \left(\frac{g_{m1k} g_{m2k}}{g_{m1k} + g_{m2k}} \right) + \left(\frac{g_{m3k} g_{m4k}}{g_{m3k} + g_{m4k}} \right), \quad (2)$$

where k is the group of g_m (k = A, B and C) and

$$g_{mik} = \sqrt{\frac{\mu C_{ox} W_i I_{Bik}}{L_i}}, \quad (3)$$

where μ is the effective carrier mobility, I_{Bk} is external DC bias current, C_{ox} is the gate-oxide capacitance per unit area, and W_i and L_i are the effective channel width and length of the transistor, respectively (where i is number of transistors = 1, 2, 3...9).

Let β be the ratio of the transconductances, where

$$\beta = \frac{v_w}{v_z} = \frac{g_{mB}}{g_{mC}}. \quad (4)$$

B. Proposed current-mode PID controller

The proposed current-mode PID controller is shown in Fig. 3(a), where its block diagram is depicted in Fig. 3(b). The proposed circuit consists of 2 VDGAs and 2 capacitors. Generally, the transfer function of the proposed current-mode controller is

$$T(s) = \frac{I_{out}(s)}{I_{in}(s)} = K_p \left[1 + \frac{1}{sT_i} + sT_d \right], \quad (5)$$

where K_p is the proportional gain, T_i is the integral time, and T_d is the derivative time. From circuit analysis of the proposed circuit in Fig. 3(a), the transfer function of the proposed VDGA-based PID controller is obtained by

$$H_{PID}(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{g_{mA2}}{g_{mC1}} \left[1 + \frac{g_{mC1}}{sC_2} + \frac{g_{mC1} sC_1}{g_{mA1} g_{mB1}} \right], \quad (6)$$

where

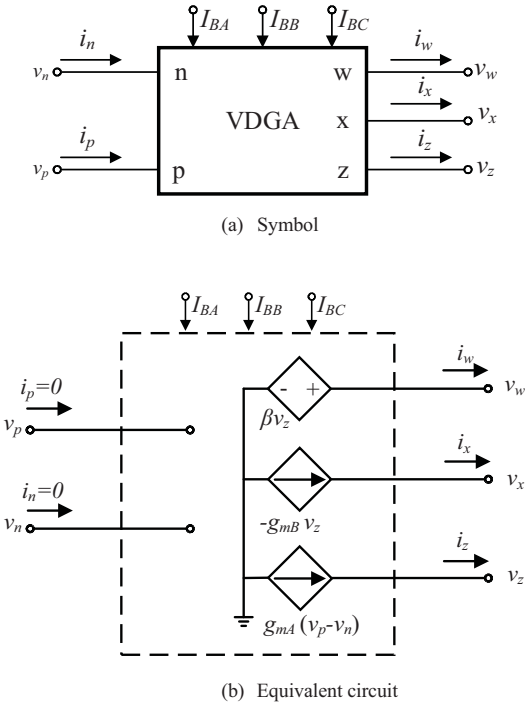
$$K_p = \frac{g_{mA2}}{g_{mC1}}, \quad (7)$$

$$T_i = \frac{C_2}{g_{mC1}}, \quad (8)$$

and

$$T_d = \frac{g_{mC1} C_1}{g_{mA1} g_{mB1}}. \quad (9)$$

From (6)-(9), the independently control parameters of the proposed PID controller can be achieved, as followed. Term of K_p can be tuned by adjusting g_{mA2}. T_i can be tuned to the required values by adjusting C_2, lastly term of T_d by adjusting C_1, g_{mA1} and g_{mB1} without effect the other terms. By the way, the proposed circuit can be electronically tuned of K_p, T_i and T_d gains, by first setting term of T_i with g_{mC1}, then setting term K_p with g_{mA1} and setting term of T_d with g_{mA1} and g_{mB1}.



(a) Symbol

(b) Equivalent circuit

Fig. 1. VDGA.

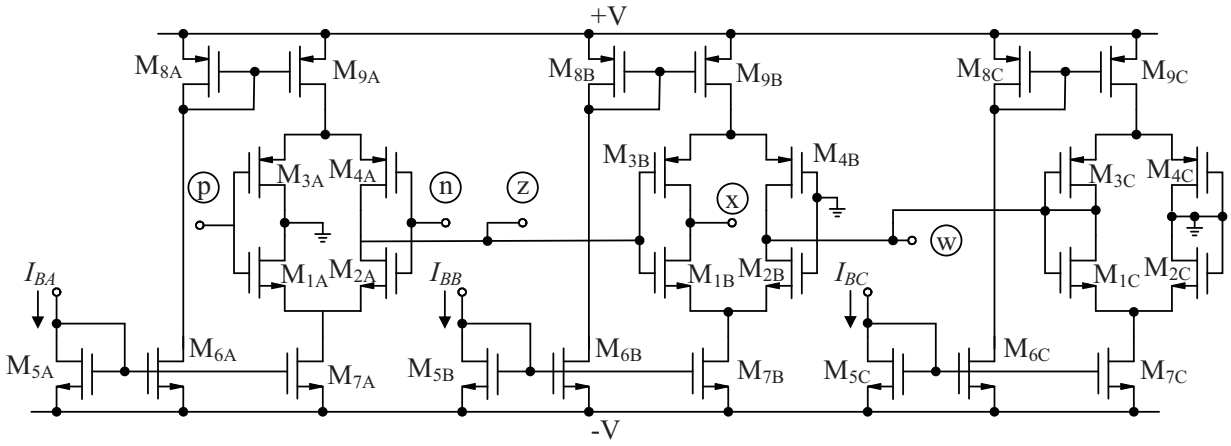
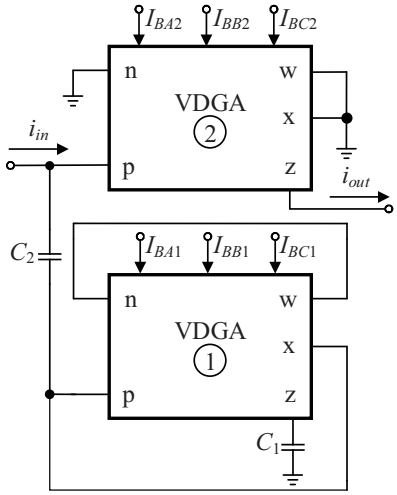
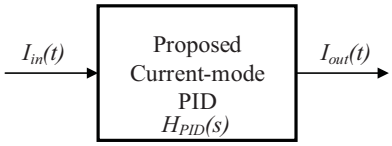


Fig. 2. CMOS implementation of the VDGA.



(a)



(b)

Fig. 3. Proposed new current-mode PID controller (a) Circuit structure (b) Block diagram.

III. NON IDEA AND SENSITIVITY

In this section, non-idea of the VDGAs will be considered. The characteristics of the VDGA terminal voltages and currents are modified to be

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \gamma_A g_{mA} & -\gamma_A g_{mA} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\gamma_B g_{mB} & 0 \\ 0 & 0 & 0 & \dfrac{\gamma_B g_{mB}}{\gamma_C g_{mC}} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_x \\ v_z \\ v_w \end{bmatrix}. \quad (10)$$

Transfer function with non-ideal consideration becomes to be

$$H_{PID}(s) = \frac{\gamma_{A2} g_{mA2}}{\gamma_{C1} g_{mC1}} \left[1 + \frac{\gamma_{C1} g_{mC1}}{sC_2} + \frac{\gamma_{C1} g_{mC1} sC_1}{\gamma_{A1}\gamma_{B1} g_{mA1} g_{mB1}} \right], \quad (11)$$

where

$$K_p = \frac{\gamma_{A2} g_{mA2}}{\gamma_{C1} g_{mC1}} \quad (12)$$

$$T_i = \frac{C_2}{\gamma_{C1} g_{mC1}} \quad (13)$$

$$T_d = \frac{\gamma_{C1} g_{mC1} C_1}{\gamma_{A1}\gamma_{B1} g_{mA1} g_{mB1}}. \quad (14)$$

Thus, the sensitivities of the pretend PID controller are

$$S_{\gamma_{A2}}^{K_p} = S_{g_{mA2}}^{K_p} = 1, \; S_{\gamma_{C1}}^{K_p} = S_{g_{mC1}}^{K_p} = -1, \quad (15)$$

$$S_{C_2}^{T_i} = 1, \; S_{\gamma_{C1}}^{T_i} = S_{g_{mA2}}^{T_i} = -1, \quad (16)$$

$$S_{\gamma_{C1}}^{T_d} = S_{g_{mC1}}^{T_d} = S_{C1}^{T_d} = 1, \quad (17)$$

and

$$S_{\gamma_{A1}}^{T_d} = S_{\gamma_{B1}}^{T_d} = S_{g_{mA1}}^{T_d} = S_{g_{mB1}}^{T_d} = -1. \quad (18)$$

TABLE I. RATIO OF CMOS TRANSISTORS

Transistors	W (μm)	L (μm)
M_{1k}- M_{2k}	16.1	0.7
M_{3k}- M_{4k}	28	0.7
M_{5k}	7	0.7
M_{6k}- M_{7k}	8.5	0.7
M_{8k}- M_{9k}	21	0.7

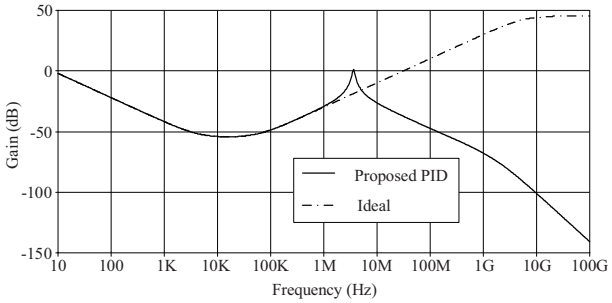
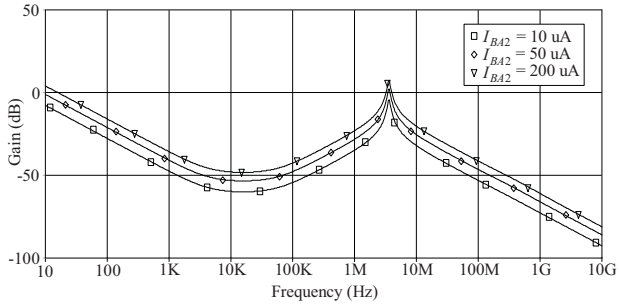
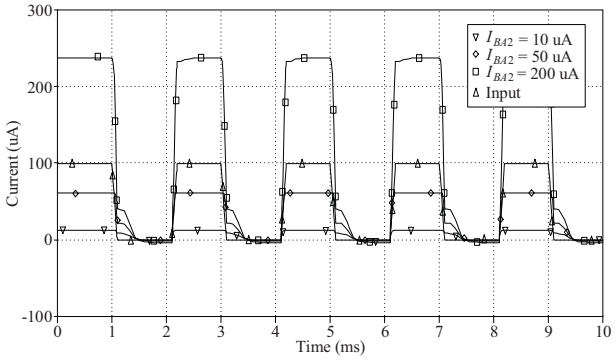


Fig. 4. Open-loop frequency response.



(a) Frequency response



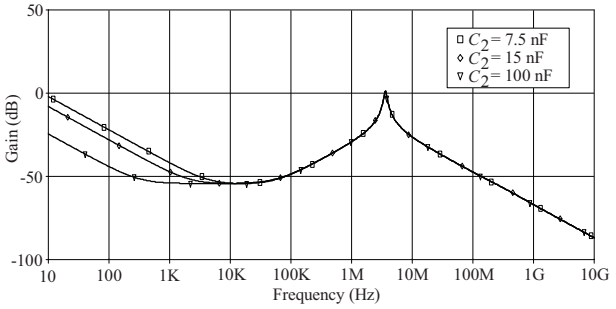
(b) Transient response

Fig. 5. K_p adjustment for different g_{mA2} (I_{BA2}).

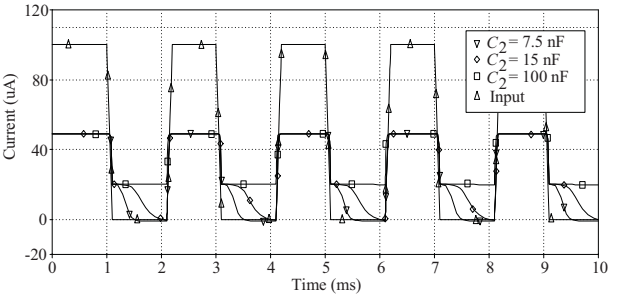
IV. SIMULATION RESULTS

The PSPICE simulation program to show performances of the proposed VDGA-based current-mode PID controller are investigated. Fig. 2 is the CMOS internal implementation of the VDGA used in the simulation, where Table. 1 is the aspect ratio of the transistors using TSMC 0.35μm [15].

Firstly, as an example, a design of open-loop PID controller by choosing C_1 = 1nF, C_2 = 7.5nF, g_{mA2} ≈ 380μA/V (I_{BA2}= 40μA), g_{mA1} ≈ 270μA/V (I_{BA1}= 20μA), g_{mB1} ≈ 270μA/V (I_{BB1}=20μA), g_{mC1} ≈ 190μA/V (I_{BC1}=10μA) and power supply of ±1.5V is performed. From these parameters, it is found that K_p ≈ 2, T_i ≈ 39.47×10^{-6}s and T_d ≈ 2.6×10^{-6}s The frequency response of open-loop operation compared to ideal frequency response is shown in Fig. 4.

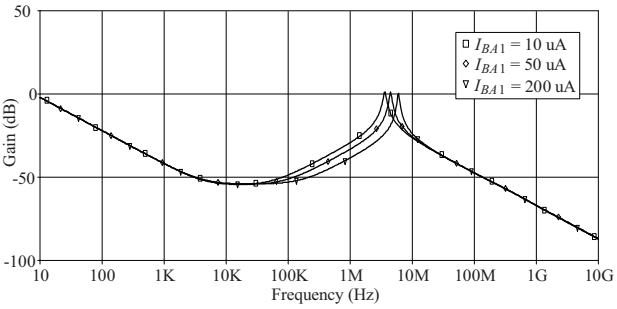


(a) Frequency response

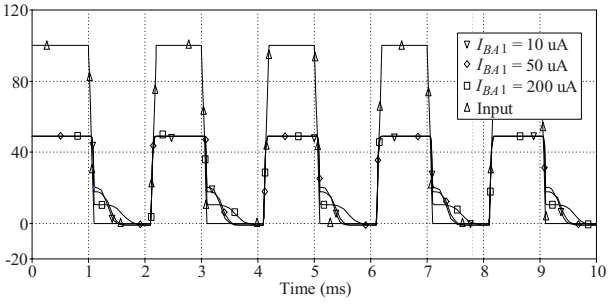


(b) Transient response

Fig. 6. T_i adjustment for different C_2.



(a) Frequency response



(b) Transient response

Fig. 7. T_d adjustment for different g_{mA1} (I_{BA1}).

Additionally, the electronic controllability of current gain; K_p by adjusting g_{mA2} (I_{BA2}) is confirmed in Fig. 5, both in frequency response and transient response. Fig. 6 also depicts adjustability of T_i of the proposed PID controller by tuning C_2. Lastly, the electronic tunability of T_d by adjusting g_{mA1} (I_{BA1}) in the PID controller is also investigated, shown in Fig. 7. By the way, the independently electronic controllability of all parameters in the proposed PID controller can be achieved by following procedure, firstly adjust g_{mC1} (I_{BC1}) to set T_i term, then assign K_p by adjusting g_{mA2} (I_{BA2}) and lastly set T_d by tuning g_{mA1} (I_{BA1}) and/or g_{mB1} (I_{BB1}).

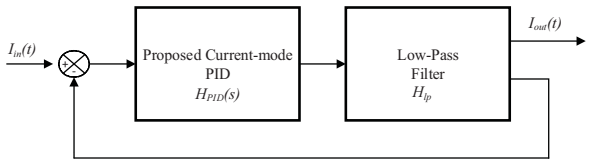
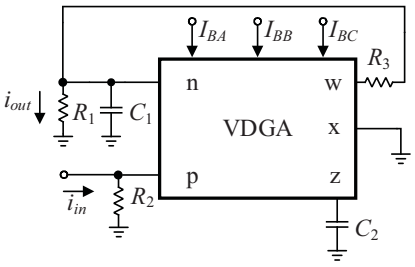
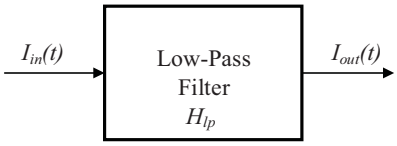


Fig. 8. Closed-loop control system.



(a) VDGA based second-order low pass filter



(b) Block diagram

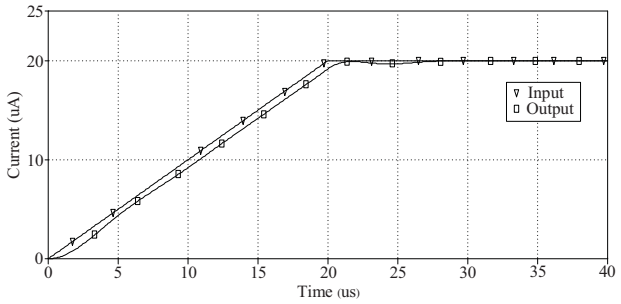
Fig. 9. A 2nd order current-mode low pass filter.

To investigate a practical workability of the proposed PID controller, a closed-loop system with a current-mode low pass filter, shown in Fig. 8, is setup. The current-mode second-order low pass filter (CM-LP) is shown in Fig. 9. Using routine analysis, the natural angular frequency (ω_O) and the quality factor (Q) of CM-LP are

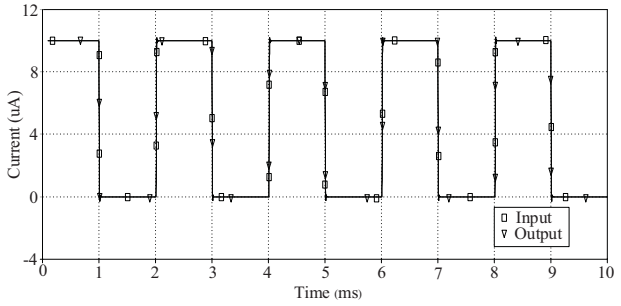
$$\omega_O = \sqrt{\frac{\beta g_{mA}}{C_1 C_2 R_3}}, \tag{19}$$

$$Q = \frac{R_1}{R_1 + R_3}\sqrt{\frac{\beta g_{mA} C_1 R_3}{C_2}}. \tag{20}$$

The circuit parameters of the low pass filter in Fig. 9 are followed; $R_1 = R_2 = R_3$ = 3kΩ, I_{BA} = 80μA, I_{BB} = 80μA, I_{BC} = 10μA and $C_1 = C_2$ = 1nF. Taking a step input with 20 μA with a 20 μs rise time and take square wave with 10μA. The following parameters of controller are assigned; K_p = 3.6, T_i = 3×10^{-6}s and T_d = 0.75 ×10^{-6}s, where I_{BA1} = 80μA, I_{BB1} = 80μA, I_{BC1} = 10μA, I_{BA2} = 160μA, I_{BB2} = I_{BC2} = 20μA, C_1 = 1nF and C_2 = 0.6nF. The transient responses of the closed-loop system for step and square wave input are shown in Fig. 10.



(a) Step response



(b) Square wave response

Fig. 10. Closed-loop system responses.

V. CONCLUSION

In this paper, a novel current mode PID controller using VDGAs has been presented. The proposed PID controller only employs 2 VDGAs and 2 capacitors. The PID controller parameters; gain K_P, K_I and K_D can be independently controlled with electronic method. The results of proposed circuit were confirmed the theoretical analysis by PSPICE simulation. The closed loop control system of PID controller and CM-LP has total power consumption approximately 5.6mW, at ±1.5V power supply. As obtained performances, it is suitable for use of the proposed VDGA-based PID controller in a control system, especially in battery-powered devices.

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