Microelectronics Reliability 87 (2018) 259–270

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Temperature effects on BTI and soft errors in modern logic circuits

W. Sootkaneung[a,*], S. Howimanporn[b], S. Chookaew[b]

[a] Department of Computer Engineering, Rajamangala University of Technology Phra Nakhon, Bangkok, Thailand
[b] Faculty of Technical Education, King Mongkut's University of Technology North Bangkok, Bangkok, Thailand

ARTICLE INFO

Keywords:
Bias Temperature Instability (BTI)
FinFET
Logic circuit
Soft error
Supply voltage
Temperature effect

ABSTRACT

Since thermal responses of the drive current in recent 3D FinFET and conventional planar transistors are different, addressing performance and reliability in advanced VLSI circuits must be reconsidered. This study investigates temperature effects on two of the most problematic reliability issues in modern logic circuits, namely Bias Temperature Instability (BTI) and soft errors. In particular, we initially examine the inversion of temperature effect that strengthens the drive current in 14-nm bulk tri-gate FinFETs with increasing temperature, and model it as a source of threshold voltage reduction. This temperature-induced threshold voltage variation is consequently adapted into our proposed simulation and analysis framework for BTI degradation in large combinational circuits. The BTI aging results from our proposed estimation are more pessimistic than that from the conventional approach where the temperature effect is excluded. Simulation results show that long-term BTI aging delay worsens as temperature increases, yet the domination of thermal effect on the drive current leads to overall performance improvement in all circuits under 10-year BTI stress. In addition, soft errors and their masking probabilities in logic circuits are addressed under the inversion of temperature effect and supply voltage variation. The results reveal that soft error immunity in all experimental circuits improves significantly with increasing supply voltage and temperature, mainly due to the increase of critical charge. The average relative soft error rate when the supply voltage changes from 0.4 V to 0.6 V and 0.8 V at 0 °C is as low as 3.7% and 0.08% of the average result at 0.4 V, respectively. On average, the relative soft error rate at a particular supply voltage when temperature changes from 0 °C to 40 °C, 80 °C, and 120 °C is around 70%, 50%, and 30% of the average result at 0 °C, respectively.

1. Introduction

In modern processors designed with 3D FinFET technology, large thermal resistance due to device structure accelerates the self-heating effect (SHE) causing a sharp increase in chip temperature [1–3]. Heat has become a major concern for most processor designers since temperature is one of the key factors that profoundly influences performance and reliability of VLSI circuits. In addition to heat issues, the response of performance to temperature variation in innovative devices is not well addressed yet, and considerably different from that of conventional transistors. Thus, previous models for temperature-dependent reliability effects may not be suitable for the state of the art technology. A few works have investigated thermal impacts on performance and reliability of FinFET devices/circuits over recent years. For device-level considerations, a physics-based thermal model for FinFET structure utilizing characteristics thermal lengths and resistances was proposed in [4]. The work in [5] observed that thermal effect on performance in SOI FinFETs is stronger than that in bulk FinFETs, but geometry and doping profiles of either of these two structures also greatly affect the thermal characteristic. Furthermore, the study in [6] suggests that the impact of process, voltage, and temperature variations on reliability of standard cells must be managed carefully at the early steps of the design. Initially addressed in [7], while the superthreshold drive current of a conventional device weakens as temperature increases, the inversion of temperature effect in a FinFET raises the drive current at high temperature. The aforementioned issue in [7] may lead to some changes in modeling performance and reliability for modern designs, and it motivates us to reconsider the thermal effect on circuit reliability.

BTI aging has been reported as one of the most serious long-term temperature-dependent reliability issues for the past and present transistor technology. Two types of BTI that affect p-type and n-type transistors are the negative BTI (NBTI) and positive BTI (PBTI), respectively. BTI causes the threshold voltage of the device to increase over time under a certain bias condition. While BTI in conventional transistors has well been studied, BTI in FinFETs has just become the focus of a few recent works. The study on BTI in SRAMs from [8] concluded

* Corresponding author.
E-mail address: warin.s@rmutp.ac.th (W. Sootkaneung).

https://doi.org/10.1016/j.microrel.2018.07.032
Received 2 March 2018; Received in revised form 11 May 2018; Accepted 3 July 2018
Available online 07 July 2018
0026-2714/

that FinFET cells are more vulnerable to BTI degradation than planar CMOS cells, and BTI is strongly dependent on supply voltage. In logic circuits, although BTI is slightly affected by supply voltage and frequency, the side effect of temperature change from dynamic voltage and frequency scaling (DVFS) is found to be increasingly significant [9]. The work in [10] developed a technique for NBTI mitigation on FinFET GPU by use of device heterogeneity that replaces more sensitive FinFETs with planar devices. In datapath logic subblocks, NBTI was found to be affected by workload and architectural factor variations [11]. A machine learning-based monitoring method was developed in [12] to estimate aging delay in embedded processers at RTL by use of BTI dependency on workload. Additionally, it was revealed in [13] that NBTI dependency on frequency is moderately serious for very high GHz applications.

On the other hand, radiation-induced soft errors have intensely affected short-term reliability of deep nanometer VLSI circuits. Particle strikes at a circuit node with sufficient energy can induce a single event transient (SET) leading to a flip in logic level. If this transient pulse can propagate through sensitized paths and reach any memory element, it will bring a soft error to the circuit. Technology scaling has exacerbated logic soft error rate (SER) to be comparable to SER of SRAMs [14, 15]. Unfortunately, managing soft errors in combinational logic requires high cost in terms of area and performance overhead [16]. For this reason, improving soft error immunity in logic circuits has become essential. While soft errors in conventional MOSFET technology have been well investigated, there have been few studies on soft errors in FinFET technology. Examples of recent works on addressing soft errors for advanced transistor technology are as follows. At the device level, the work in [17] modeled SET in advanced devices and ICs for various design structures. Furthermore, the study in [18] proposed a technique to improve soft error rate (SER) by adjusting some geometrical parameters of individual FinFETs. The results from [19] reveal that soft error vulnerability of FinFETs is significantly lower than that of the prior technologies. In [20], soft errors in SRAMs and logic circuits, designed with different device materials and architectures, were evaluated under supply voltage scaling. For FinFET flip-flop and SRAMs, the impact of process variation in smaller technology nodes and influence of supply voltage on SER are substantially powerful [21–23]. In [24], the assessment of logic SER and flip-flop SER for alpha particle strikes in 28-nm circuits was performed considering the impact of supply voltage and frequency. Performance of SET hardening strategies was analyzed in [15] for FinFET and planar circuits operating at near-threshold voltage under the impact of technology scaling as well as the variations in threshold voltage and supply voltage.

Most of the previous works on BTI and soft errors in FinFETs exploited reliability models for conventional planar technology, regardless of the thermal impact. These include the recent investigations for the impact of BTI on logic SER in [25, 26]. On the other hand, our preliminary study [27] noticed that the inversion of temperature effect in modern designs that improves circuit performance at high temperature provides positive feedback of heat and larger BTI degradation. This also motivates us to further investigate the thermal impact on BTI and soft error masking characteristics in FinFET designs. In this work, we show an effort to address impacts of temperature on BTI aging and soft errors in logic circuits. The contributions of our study are as follows.

1) Addressing BTI in FinFET combinational circuits considering thermal impact:

We propose and verify the idea of representing thermal response of the drive current and delay as a source of threshold voltage variation. This temperature-induced threshold voltage shift is taken in evaluating thermal effect on BTI degradation in large combinational circuits.

2) Evaluating logic soft errors under temperature effect and circuit parameter variations:

We investigate the impact of temperature on soft error masking probabilities and logic SER. The proposed simulation and analysis framework of thermal response of soft errors takes supply voltage variation into consideration.

The remainder of this paper is organized as follows. A brief review of temperature effect on the drive current and delay in FinFET devices and logic gates is provided in Section 2. Effect of temperature on BTI aging is discussed in Section 3. Section 4 discusses thermal impact of soft errors under circuit parameter variation and BTI aging. Finally, all works are concluded in Section 5.

2. Temperature effects on circuit performance

This section reviews the impact of temperature on the drive current of FinFET devices and delay performance of logic gates. We also discuss a temperature-dependent delay model in which the temperature effect is considered as another source of threshold voltage variation. Finally, the proposed delay model is used to investigate the delay of large benchmark circuits designed with FinFET technology under temperature variation.

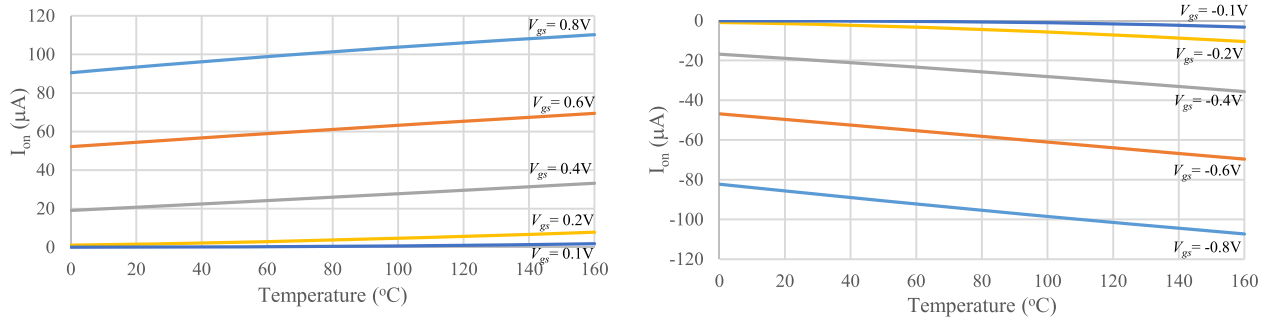
2.1. Inversion of temperature effect in FinFETs

Two key temperature-dependent parameters that affect the drive current of a transistor are carrier mobility and threshold voltage. The degradation of mobility at high temperature significantly impacts conventional planar transistors due to the ionized impurity and phonon scattering effect from their highly doped body to mitigate the short-channel effect [28]. On the other hand, more intrinsic FinFET's body causes the carrier mobility to be relatively insensitive to temperature variation. Although threshold voltage of both devices tends to decrease with temperature, high tensile stress in FinFET's thin body induces the bandgap narrowing that consequently results in large threshold voltage reduction [29]. Hence, with increasing temperature, FinFETs experience the stronger drive current.

The drive current (I_{on}) of both types of transistor in subthreshold and superthreshold regimes can be expressed as

$$I_{on} = \begin{cases} \mu(T) e^{\frac{V_{gs} - V_{th}(T)}{S(T)}}, & V_{gs} < V_{th} \\ \mu(T)(V_{gs} - V_{th}(T))^{\alpha}, & \text{otherwise} \end{cases} \quad (1)$$

where μ, S, V_{th}, and α are the carrier mobility, subthreshold swing, threshold voltage, and velocity saturation index, respectively [7]. Fig. 1 plots I_{on} with temperature in a 14-nm bulk tri-gate nFinFET (Fig. 1(a)) and pFinFET (Fig. 1(b)) for different V_{gs} levels, whereas Fig. 2 illustrates the temperature effect on I_{on} in a 22-nm high-k/metal gate nMOSFET (Fig. 2(a)) and pMOSFET (Fig. 2(b)). It can be noticed from Fig. 1 and Fig. 2 that in subthreshold operation with small V_{gs}, I_{on} of both planar and 3D transistors increases as temperature increases because the increase of the exponential term in (1) mainly due to heat-induced V_{th} reduction dominates the change of μ-dependent term. However, in superthreshold operation with large V_{gs}, I_{on} of both types of transistor reacts to temperature differently. The planar device has weaker I_{on} with increasing temperature because the large degradation in $\mu(T)$ overrides the nearly linear increase of the V_{th}-dependent term. On the other hand, the slight change in $\mu(T)$ of the FinFET cannot supersede the impact of its decreased V_{th}, thereby strengthening the superthreshold I_{on}. Therefore, at high temperature in superthreshold operation, the stronger drive current in FinFETs improves timing performance of the chip whereas the weaker I_{on} in planar MOSFETs leads to performance degradation.



(a) nFinFET (b) pFinFET

Fig. 1. I_{on} with temperature in 14-nm bulk tri-gate n/pFinFETs for different V_{gs}.

2.2. Temperature-induced variations in threshold voltage and circuit delay

Threshold voltage variation predominantly influences various performance- and reliability-related issues. A shift in threshold voltage can cause a device to run faster (lower V_{th}) or slower (higher V_{th}). The variation in gate and flip-flop timing performance can consequently affect some masking probabilities that define SER of a circuit. In addition, the devices with low V_{th} tend to have larger BTI stress than those high-V_{th} transistors at a particular temperature [27]. The concern about threshold voltage variation has commonly been raised in modeling a number of performance and failure mechanisms.

To take into account the effect of temperature, we consider the temperature variation equivalent to the threshold voltage shift from the reference level at a fixed temperature. Fig. 3 shows the equivalent threshold voltage shift due to temperature ($\Delta V_{th,Temp}$) that causes the device drive current to change around the reference temperature of 25 °C with $|V_{gs}| = 0.8$ V for 14-nm tri-gate n/pFinFETs (Fig. 3(a)) and 22-nm high k/metal gate planar n/pMOSFETs (Fig. 3(b)). The increase in the drive current of the FinFETs at higher temperature in Fig. 3(a) is captured by the decrease in their threshold voltage at 25 °C (negative $\Delta V_{th,Temp}$). On the other hand, the threshold voltage of planar MOSFETs in Fig. 3(b) increases with temperature (positive $\Delta V_{th,Temp}$) weakening the device drive current. The alpha-power law [10] stated below can be adopted to estimate the circuit delay.

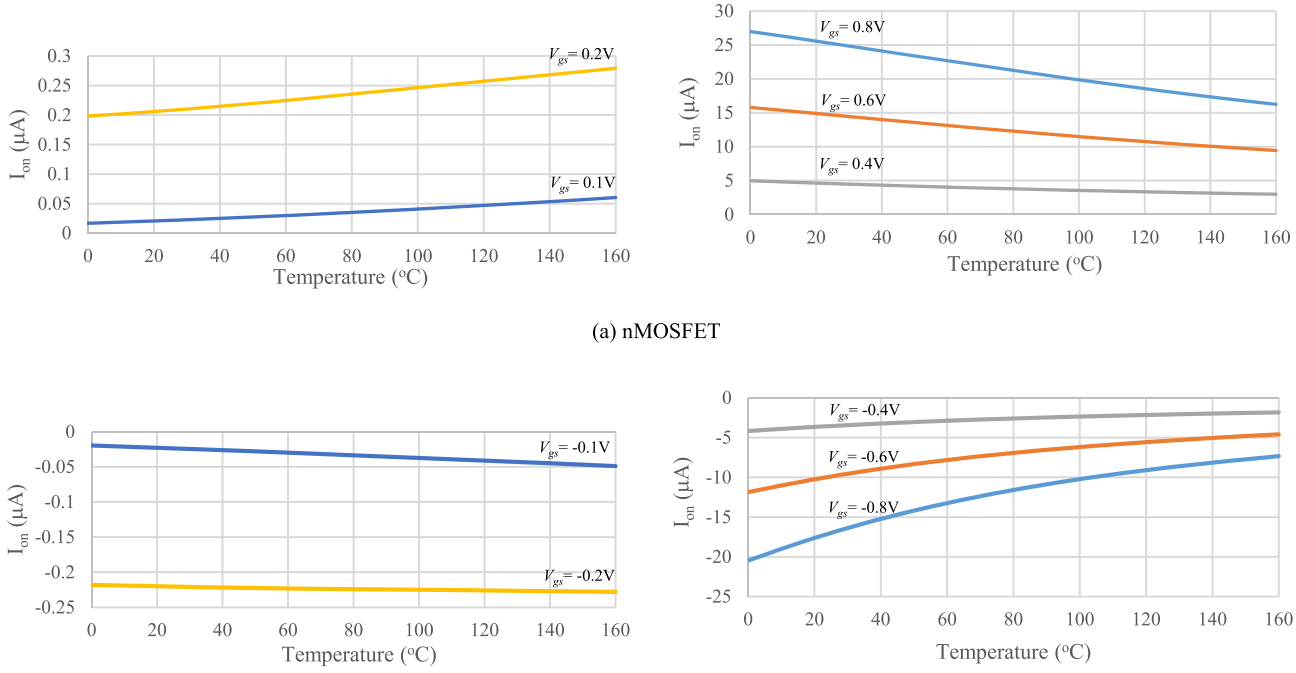
$$delay \propto \frac{V_{dd}}{[V_{dd} - (V_{th0} + \Delta V_{th,Temp})]^{\alpha}} \tag{2}$$

where α is the velocity saturation index, V_{dd} is the supply voltage, and V_{th0} is the original threshold voltage. From (2), the negative $\Delta V_{th,Temp}$ for FinFETs causes the transistor delay to decrease with increasing temperature, whereas the positive $\Delta V_{th,Temp}$ at high temperature for planar devices worsens their timing performance. In the general case where other causes of threshold voltage variation take place, the shift in threshold voltage for each individual transistor is likely to be different. Under the shift in threshold voltage $\Delta V_{th,\,i}$ corresponding to transistor i, the simplified form of (2), which gives the change in the delay of transistor i ($\Delta t_{d,\,i}$) [30, 31], can be expressed as

$$\Delta t_{d,i} = \frac{\alpha \Delta V_{th,i}}{V_{dd} - V_{th0}} t_{d0,i} \tag{3}$$

where $t_{d0,\,i}$ is load-dependent original delay. It can be noticed from (3) that with a given load, $\Delta t_{d,\,i}$ is proportional to $\Delta V_{th,\,i}$.

For a parallel transistor network, the worst-case network delay is defined as the delay of the transistor with the smallest decrease or the



(a) nMOSFET

(b) pMOSFET

Fig. 2. I_{on} with temperature in 22-nm high k/metal gate n/pMOSFETs for different V_{gs}.

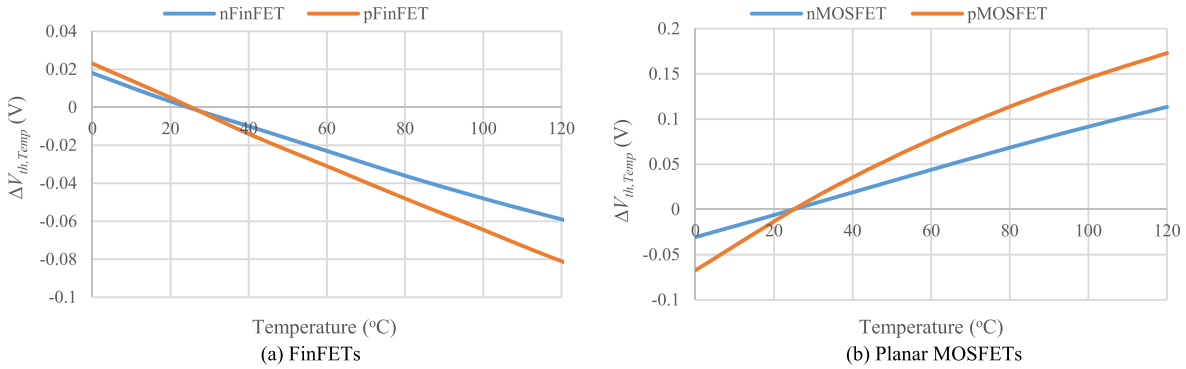


Fig. 3. $\Delta V_{th,Temp}$ of 14-nm bulk tri-gate n/pFinFETs and 22-nm high k/metal gate n/p planar MOSFETs with V_{gs} = 0.8 V.

largest increase in threshold voltage. That is

$$\Delta t_{d,par} = C_{par} \bullet t_{d0} \bullet \max\{\Delta V_{th,i}\} \tag{4}$$

where $\Delta t_{d,\ par}$ is the change in the delay of the parallel transistor network, t_{d0} is the original network delay, and the proportional constant C_{par} can be identified by linear fitting. Particularly, all constants in (4) can be determined under the assumption that the original network delay is considered proportional to intrinsic capacitance and load capacitance. Both types of capacitance can be estimated linear with the total number of fins of transistors connected to the gate output as fully discussed and verified in [32].

For a series network, each device contributes to the change in the network delay $\Delta t_{d,\ ser}$, which is given by

$$\Delta t_{d,ser} = \sum_{i=0}^{\#of\ inputs-1} \Delta t_{d,i} \tag{5}$$

where

$$\Delta t_{d,i} = C_{ser} \bullet t_{d0,i} \bullet \Delta V_{th,i} \tag{6}$$

The constant C_{ser} and original delay $t_{d0,\ i}$ in (6) can be obtained from the linear relationship between $\Delta V_{th,\ i}$ and $\Delta t_{d,\ i}$ at a particular load capacitance [32]. As we focus on the temperature effect on timing performance of the circuit under BTI stress, the total $\Delta V_{th,\ i}$ consists of $\Delta V_{th,\ Temp}$ and the threshold voltage shift due to BTI aging.

The gate propagation delay under threshold voltage variation can be achieved by averaging the values of falling and rising propagation delay of parallel and series networks in (4) and (5). Further, we can perform critical path analysis to evaluate the overall circuit delay. An advantage of using this proposed delay model is that we simply keep the operating temperature constant, while varying the corresponding $\Delta V_{th,\ Temp}$.

2.3. Model verification

Considering that the threshold voltage shift is caused by only temperature effect, all n or p transistors operating at a particular temperature have the same amount of threshold voltage variation which is equal to $\Delta V_{th,Temp}$. The idea of using $\Delta V_{th,Temp}$ to match the change in circuit delay due to temperature effect was initially applied to evaluate the delay of all mapping gates in the cell library which consists of the inverter and 2-, 3- 4-input NAND/NOR gates designed with the 14-nm bulk tri-gate FinFET predictive technology from [33]. The proposed delay estimation primarily uses (4)–(6) assuming that the operating temperature is fixed at 25 °C, while the threshold voltage of each type of transistor is varied by $\Delta V_{th,Temp}$. We compared the proposed delay model with the reference SPICE model where temperature was adjusted directly. The comparison shown in Fig. 4(a) – (g) was performed for each library gate with the nominal superthreshold supply voltage of 0.8 V and the same given load. As reported in Fig. 4, the proposed method yields the outcomes that are very close to those from the temperature-dependent SPICE model for all types of gate in the cell library. Therefore, use of $\Delta V_{th,Temp}$ to capture the temperature variation is reasonably applicable. A more effort may be taken if we derive the gate/circuit delay directly from temperature variation.

Further, we applied our proposed delay model to large circuits selected from ISCAS-85/89 (combinational parts) and MCNC benchmark suites to investigate the delay characteristic of FinFET designs under temperature variation. The library gates for all experimental circuits include all gates that were evaluated in Fig. 4 with 0.8-V supply voltage. In this simulation and analysis of delay performance, the temperature variation is represented as the shift in threshold voltage $\Delta V_{th,Temp}$ from the reference level at 25 °C as illustrated in Fig. 3. Table 1 reports the normalized delay results with respect to the delay at 25 °C for a number of logic circuits operating under different temperatures (40 °C, 80 °C, and 120 °C). It is clearly seen that the inversion of temperature effect causes all experimental circuits in Table 1 to run faster as temperature increases. It can also be noticed from Table 1 that the average delay of all circuits reduces as large as 19% when the operating temperature changes from 25 °C to 120 °C. The results in Table 1 remind us of the importance of the inversion of temperature effect in FinFET designs where the moderate influence of temperature cannot be excluded from modeling and analysis of the circuit delay. The increase of the drive current with temperature essentially affects not only the performance but also the reliability of FinFET designs. Unfortunately, few works have thoroughly investigated the latter, leaving reliability analysis in modern VLSI circuits relatively inaccurate. As BTI and soft errors have increasingly worsened long-term and transient reliability of the state of the art processors in recent years, thermal response of FinFET motivates us to further develop better models for the above problems.

3. Temperature effect on BTI

BTI related theories are briefly described in this section. Afterwards, long-term BTI degradation under temperature effect in large experimental circuits is investigated considering temperature-induced threshold voltage variation.

3.1. BTI background

NBTI and PBTI gradually downgrade the drive current of p-type and n-type devices over time. A p-type transistor suffers NBTI stress under the negative bias where holes from the inversion layer break Si—H bonds at the Si/SiO_2 interface generating dangling Si^+ bonds (also known as the interface traps) and H diffusion from the interface. These interface traps cause an increase in device threshold voltage, thereby weakening the drive current. When the negative bias is terminated, some of H atoms diffuse back and passivate the interface traps resulting in the recovery of device threshold voltage. PBTI that affects n-type devices is caused by electron trapping in high-k dielectrics. The

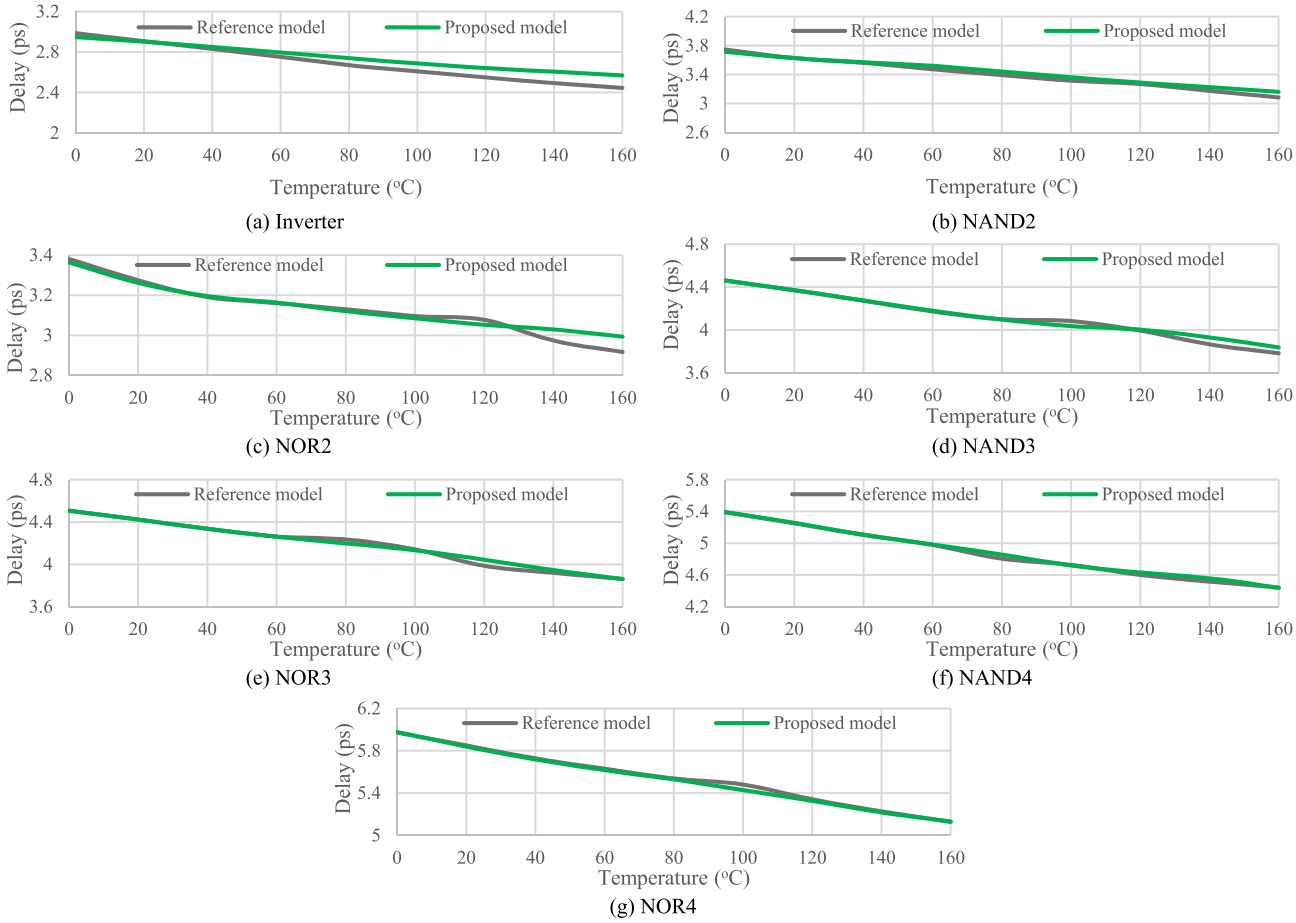


Fig. 4. Delay model verification for each mapping gate in the cell library.

Table 1
Normalized delay under temperature variation.

Circuit	Normalized delay		
	40 °C	80 °C	120 °C
C1908	0.9692	0.8909	0.8177
C6288	0.9699	0.8927	0.8197
C7552	0.9722	0.9021	0.8371
i7	0.9733	0.9065	0.8456
i8	0.9597	0.8554	0.7555
i9	0.9683	0.8872	0.8104
S5378	0.9721	0.9020	0.7375
S15850	0.9732	0.9061	0.8445
S35932	0.9747	0.9121	0.8557
Average	0.9703	0.8950	0.8137

fabrication process and quality of the high-k material considerably influence PBTI degradation [34].

A reaction-diffusion (RD) based BTI model for long-term V_{th} shift prediction [35, 36] can be expressed as

$$\Delta V_{th,BTI} = \chi \left(\frac{\sqrt{[K_s(C,Q_{inv})]^2 \bullet s \bullet t_{cycle}}}{1 - [K_r(C,t)]^{(1/2n)}} \right)^{2n} \tag{7}$$

where $\Delta V_{th,\ BTI}$ is the threshold voltage shift due to BTI in a transistor, χ is set to 1 for NBTI and 0.5 for PBTI, $K_s(C, Q_{inv})$ and $K_r(C, t)$ are the parameters of stress and recovery mechanisms, respectively, s is the fraction of stress time, t is the operating time, t_{cycle} is the stress/recovery cycle time, and n is the fitting parameter which is either 1/4 for H-based diffusion or 1/6 for H_2-based diffusion.

$K_s(C, Q_{inv})$ is a function of the diffusion temperature-dependent coefficient (C) and inversion charge density (Q_{inv}) which are defined by the following equations [37].

$$C = T_0^{-1} exp\left(\frac{-E_a}{k_B T}\right) \tag{8}$$

where E_a is the activation energy, k_B is the Boltzmann's constant, and T_0 is another temperature-related constant, and

$$Q_{inv} = C_{ox}(V_{gs} - V_{th}) \tag{9}$$

where Q_{inv} is the inversion charge density for saturation region which is bias-dependent, and C_{ox} is the gate capacitance per unit area. In addition to the parameter of stress, the parameter of recovery, $K_r(C, t)$, is time-dependent and is also a function of C.

All parameters in (7), (8) and (9) are adopted from [35, 38]. To sum up, the threshold voltage shift due to BTI or $\Delta V_{th,\ BTI}$ in (7) that causes the circuit delay to increase over time is dependent on temperature, time, bias, and original threshold voltage.

3.2. BTI under temperature effect

For a FinFET device, increased temperature exponentially increases the temperature-dependent term in (8), and moderately raises Q_{inv} in (9) due to threshold voltage reduction by $\Delta V_{th,Temp}$. Furthermore, the term Q_{inv} is bias-dependent where each level of V_{gs} has a strong influence on it. This study comprehensively takes into account the dependence of BTI stress on the input vectors and device position that provide different levels of V_{gs} for each transistor in the gate. Let P_{stress} be the probability that the device is under stress (input logic level "0" for pFinFET NBTI or "1" for nFinFET PBTI), and $P_{s,\ j}$ be the probability that

Table 2
BTI degradation results after 10-year operation from the proposed model and conventional model.

Circuit	Delay increase (%)*					
	40 °C		80 °C		120 °C	
	BTI with $\Delta V_{th,Temp}$	BTI without $\Delta V_{th,Temp}$	BTI with $\Delta V_{th,Temp}$	BTI without $\Delta V_{th,Temp}$	BTI with $\Delta V_{th,Temp}$	BTI without $\Delta V_{th,Temp}$
C1908	1.47	1.43	2.78	2.51	4.73	3.98
C6288	1.48	1.44	2.84	2.56	4.91	4.13
C7552	1.43	1.39	2.66	2.40	4.46	3.75
i7	1.37	1.33	2.53	2.29	4.22	3.54
i8	1.80	1.75	3.54	3.20	6.35	5.33
i9	1.70	1.65	3.27	2.95	5.68	4.77
S5378	1.36	1.32	2.53	2.29	4.26	3.58
S15850	1.25	1.22	2.32	2.10	3.87	3.25
S35932	1.35	1.31	2.46	2.23	4.05	3.41
Average	1.47	1.43	2.77	2.50	4.73	3.97

* Results are compared to BTI-free delay at each operating temperature.

the device is under stress level j corresponding to $V_{gs,\,j}$. $P_{s,\,j}$ indicates that some transistors in the stack may experience weaker stress ($|V_{gs}| \le V_{dd}$) even though they have input logic level "0" for pFinFETs or "1" for nFinFETs. Long-term threshold voltage shift due to BTI in transistor i with bias level j, considering temperature effect, can be obtained from the following equation.

$$\Delta V_{th,BTI,i} = \sum_{j=1}^{\#\,of\ stress\ levels} \left(\frac{P_{s,j}}{P_{stress}}\right) \bullet \Delta V_{th,BTI}(C, Q_{inv,j}) \tag{10}$$

where

$$Q_{inv,j} = C_{ox}\left[V_{gs,j} - (V_{th} + \Delta V_{th,Temp})\right] \tag{11}$$

BTI stress in FinFET circuits with negative $\Delta V_{th,\,Temp}$ tends to be strong according to (11). To evaluate delay degradation due to BTI in conjunct with temperature effect, the summation of $\Delta V_{th,\,BTI,\,i}$ and $\Delta V_{th,\,Temp,\,i}$ represents the total change in threshold voltage of each individual device i or $\Delta V_{th,\,i}$ in (4), (5), and (6). BTI degradation in the same experimental circuits as described in the previous section is analyzed in this simulation. All experimental circuits operate at 2-GHz frequency, and the delay degradation results are evaluated after 10-year BTI stress. Table 2 compares BTI-induced delay degradation predicted by the proposed approach that takes $\Delta V_{th,\,Temp}$ into account and the conventional model where the inversion of temperature effect is neglected. The increase in long-term delay reported in Table 2 is compared to the original delay of the circuits at each operating temperature. Each baseline delay at 40 °C, 80 °C, and 120 °C is computed regardless of BTI degradation. It can be clearly seen in Table 2 that the performance degradation due to BTI aging resulted from the proposed approach is moderately high compared to the estimation from the reference approach. Since we take $\Delta V_{th,\,Temp}$ in BTI evaluation, the negative value of $\Delta V_{th,\,Temp}$ due to the inversion of temperature effect subsequently raises $Q_{inv,\,j}$ in (11) leading to large BTI degradation compared to the results from the reference method. Furthermore, BTI aging delay estimated by both approaches tends to increase as the baseline temperature increases.

Although the relative BTI stress is higher as the baseline temperature increases, the inversion of temperature effect is found to be stronger than the impact of long-term BTI aging. Fig. 5 shows the normalized delay of the circuit C1908 under BTI and no BTI while the operating temperature is varied. To investigate BTI aging under temperature variation, all points on the plots in Fig. 5 are normalized with respect to the original BTI-free delay at the fixed temperature of 25 °C (on the "No BTI" line at 25 °C). We can notice from the "With BTI" line in Fig. 5 that increased temperature still gives the improvement of

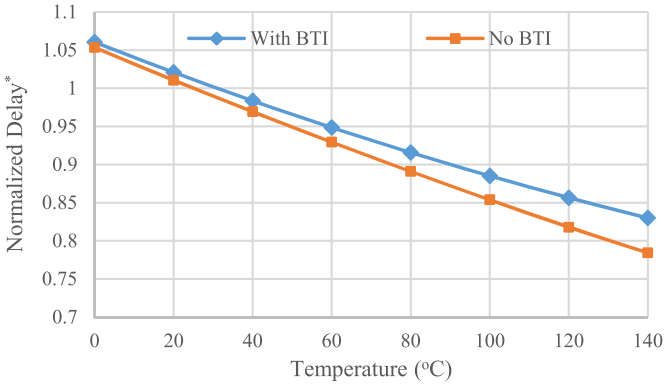


Fig. 5. Timing performance improvement with temperature for the circuit C1908 under 10-year BTI stress and without BTI.
*Delay results are normalized with respect to BTI-free results at 25 °C.

timing performance of the circuit even though it has been under BTI stress for 10 years. The delay for both conditions always decreases linearly with temperature, but the rate of the decrease in the circuit under BTI is smaller. Therefore, the difference of the delay between two traces in Fig. 5 is larger at the higher temperature. At a particular temperature, the ratio of the gap between the two traces to the value on "No BTI" line provides the same comparative results as reported in the first column of each operating temperature in Table 2.

While it has been found in various studies that BTI aging in logic circuits is not highly sensitive to supply voltage and frequency variations, our investigation has just revealed that BTI is also slightly affected by temperature variation. Considering BTI stress, all circuits still have performance improvement at higher temperature. The inversion of temperature effect in modern VLSI circuits predominately causes the negative $\Delta V_{th,\,Temp}$ as temperature increases that override the positive $\Delta V_{th,\,BTI}$. However, heat in FinFET designs has been raised in a number of research studies as one of the major factors of reliability degradation that must be properly managed. In addition to BTI, the impact of temperature on soft errors will be discussed in the next section.

4. Temperature effect on soft errors

The analysis framework of this study includes evaluating soft errors in some large logic circuits under temperature and supply voltage variation. We firstly review soft error background and thermal impact on soft error masking probabilities. Then, we discuss the proposed gate-level simulation methodology to address soft errors in large circuits. We finally provide the analysis results and some interesting remarks.

4.1. Soft error background

A transient pulse from particle strikes at a single node in a gate or single event transient (SET) current can be modeled as a double exponential current given by

$$I(t) = \frac{Q_{dep}}{\tau_2 - \tau_1}\left(e^{\frac{-t}{\tau_2}} - e^{\frac{-t}{\tau_1}}\right) \tag{12}$$

where Q_{dep} is the amount of charge deposition at the active node and τ_1 and τ_2 are the rise and fall time constants, respectively [22]. We consider the drain of each transistor the active node for the strike. If the charge collection is higher than the critical charge (Q_{crit}), the strike potentially causes a flip in gate output logic. If this transient pulse is finally latched into a flip-flop, it brings a miscalculation called a soft error to the circuit. The rate of which soft errors arise in the circuit or soft error rate (SER) depends on the rate of SET generation due to particle strikes and various masking probabilities along propagation paths. SER for a strike at transistor i in the gate can be expressed by the

following equation.

$$SER_i = \varphi \bullet A_{active,i} \bullet P_{SET,i} \bullet P_{Elec,i} \bullet P_{Logic,i} \bullet P_{Latch,i} \quad (13)$$

where φ is the particle flux and $A_{active,\ i}$ is approximately the drain area of transistor i where the strike happens. The probabilities $P_{SET,\ i}$, $P_{Elec,\ i}$, $P_{Logic,\ i}$, and $P_{Latch,\ i}$ are the SET generation, electrical, logical, and latching-window masking probabilities, respectively, corresponding to the SET that is initially generated and propagated from transistor i. To perform comparative analysis, the particle flux is considered as a constant.

The SET generation probability for transistor i, $P_{SET,i}$, is related to the transistor Q_{crit} and the average charge collected at the vulnerable area as given in (14) below [21, 22].

$$P_{SET,i} = exp\left(\frac{-Q_{crit,i}}{\eta}\right) \quad (14)$$

In the above equation, η is the charge collection efficacy which is proportional to the product of the linear energy transfer (LET) for neutrons hitting silicon and the length of the particle path through the active area (L_c) [39]. LET for silicon at sea level is estimated to 50 fC/μm, and L_c extends from 5 nm to 50 nm depending strongly on device geometry [20].

The electrical masking probability, $P_{Elec,i}$, exhibits the attenuation of the transient pulse while propagating from transistor i through several stages of logic gates to latch elements. A SET pulse in small nanometer designs is hardly attenuated thanks to their low node capacitance, causing $P_{Elec,i}$ to be very high (assumed to be 1 in this study). The logical masking probability, $P_{Logic,i}$, is dependent on the input combinations and circuit topology where SET propagated from transistor i may be blocked logically. Both $P_{Elec,i}$ and $P_{Logic,i}$ are relatively insensitive to temperature change [24]. Additionally, the latching-window masking probability, $P_{Lacth,i}$, is the probability that the SET from transistor i arrives within setup and hold time window of flip-flops. $P_{Lacth,i}$ can be expressed as

$$P_{Latch,i} = \frac{PW_i - t_{S-H}}{t_{Clk}} \quad (15)$$

where PW_i is the SET pulsewidth generated at transistor i, $t_{S\text{-}H}$ is the setup and hold time window, and t_{Clk} is the clock cycle time [24].

4.2. Impact of temperature on SET

The variation of temperature in FinFET designs has a considerable influence on Q_{crit} that exponentially affects P_{SET} in (14). Interestingly, Q_{crit} of a FinFET gate, induced by a neutron strike under temperature variation, is remarkably different from that of a planar MOSFET gate. Fig. 6 compares the plots of the neutron strike Q_{crit} at the pull-up node (pMOS) of a minimum size inverter designed with 14-nm bulk FinFETs (#of fins of both pFinFET and nFinFET = 1) and 22-nm high-k/metal gate MOSFETs (W_p/W_n = 2/1) with an FO4-inverter load and the supply voltage of 0.8 V. In this situation, the strike with sufficient energy can turn on the pMOS and flip the output logic level from "low" to "high". In general, Q_{crit} of FinFET devices in Fig. 6 tends to be larger than that of planar transistors thanks to their superior electrical integrity providing higher robustness against the charge deposition from particle strikes. The results of temperature effect on Q_{crit} in Fig. 6 reveal that Q_{crit} of the FinFET inverter increases linearly with temperature, while the other decreases. These opposite thermal responses of Q_{crit} of both designs are predominantly caused by the temperature effect on the drive current. At high temperature, the stronger drive current of FinFETs due to the inversion of temperature effect can rapidly dissipate the deposited charge from the strike. Thus, FinFET designs can tolerate higher strike energy as temperature increases, or in other words, larger amount of critical charge deposition Q_{crit} is required to generate the SET current. The contrary thermal reaction in planar devices where the

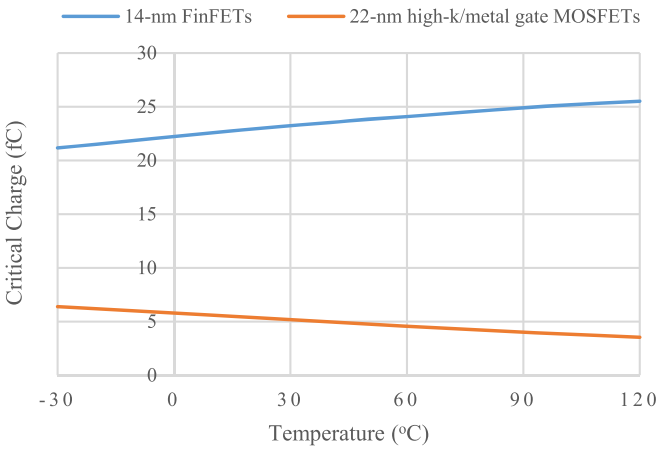
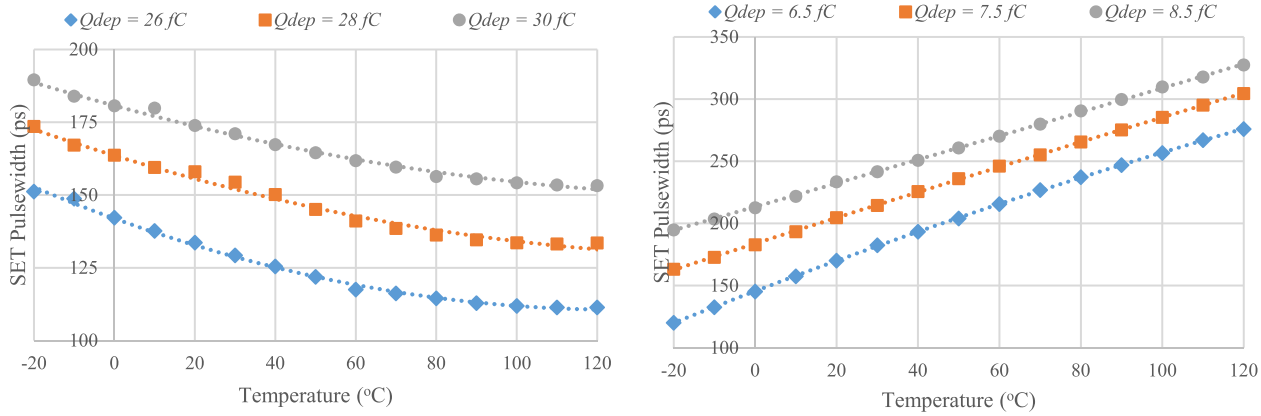


Fig. 6. Critical charge vs. temperature for a neutron strike at the pull-up node of an inverter designed with 14-nm bulk tri-gate FinFET and 22-nm high-k/metal gate MOSFET technologies.

increased temperature weakens the drive current causes their Q_{crit} to decrease with increasing temperature. According to (14), P_{SET} and Q_{crit} have a negative exponential relationship. Therefore, P_{SET} of FinFET circuits tends to decrease with temperature, whereas P_{SET} of conventional designs responds oppositely. In addition, because η in (14) is weakly influenced by temperature variation [40], η is considered insensitive to temperature in this work.

The pulsewidth of the SET current has a strong influence on P_{Latch} in (15). Two main factors that vary the SET pulsewidth are energy of the strike and circuit variation (such as node capacitance, voltage, and temperature). For a particle strike with higher energy, SET current with larger pulsewidth can be generated. If we consider temperature variation, the thermal response in silicon can further either strengthen or diminish the SET pulsewidth. Fig. 7 compares impacts of charge deposition and temperature on pulsewidth of the SET appearing at the output of an inverter designed with the 14-nm bulk tri-gate FinFET technology (Fig. 7(a)) and 22-nm high k/metal gate planar technology (Fig. 7(b)). The SET current injection for both designs occurs at the pull-up device with $Q_{dep} > Q_{crit}$ to ensure the flip-up of the output logic. The larger amount of charge deposited implies that the strike has higher energy. In Fig. 7(a) and (b), the larger amount of Q_{dep} from the strike at a particular temperature generally provides the wider SET pulsewidth in both designs. However, as temperature increases, the strike in the FinFET inverter in Fig. 7(a) generates a narrower SET pulse, whereas the planar gate in Fig. 7(b) experiences a wider SET pulse. These remarks can be explained as follows. At high temperature, the inversion of temperature effect in the FinFET gate raises the drive current that delivers fast dissipation of charge deposition and results in the decrease of SET pulsewidth. On the other hand, since the planar inverter loses its driving capability with increasing temperature, its poorer dissipation of charge deposited from the strike causes SET pulsewidth to increase.

In most soft error simulations, wide-range charge injection for $Q_{dep} \geq Q_{crit}$ is required to precisely capture the values of the generated SET pulsewidth for different strike energy. To simplify this, we define the minimum pulsewidth (PW_{Min}) which is the SET pulsewidth at the threshold condition that the strike has enough energy to exactly generates $Q_{dep} = Q_{crit}$. The lowest strike energy that can generate the narrowest SET pulse gives the lower bound of P_{Latch} ($P_{LatchMin}$) according to (15). In this study, we use PW_{Min} to evaluate $P_{LatchMin}$ for all experimental circuits. Further, the corresponding $P_{LatchMin}$ for each strike is used to assess the lower bound of SER. Fig. 8 plots PW_{Min} and temperature in the same inverter designed with FinFET technology (Fig. 8(a)) and planar technology (Fig. 8(b)). Unlike the simulation shown in Fig. 7 where the thermal impact of Q_{crit} is neglected (in Fig. 7, we always kept injected Q_{dep} larger than Q_{crit} at each temperature



(a) FinFET inverter (b) Planar MOSFET inverter

Fig. 7. SET pulsewidth vs. temperature in an inverter with different charge deposition for (a) 14-nm bulk tri-gate FinFET technology and (b) 22-nm high-k/metal gate MOSFET technology.

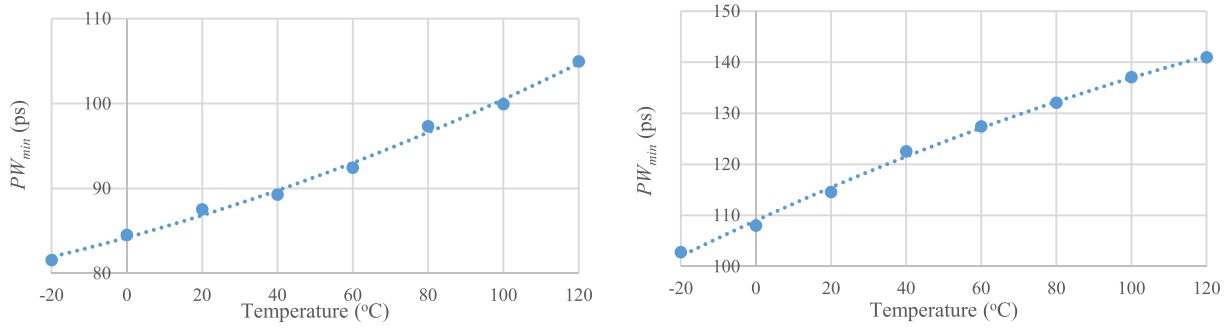
point), the amount of injected Q_{dep} to obtain PW_{Min} in Fig. 8 is set to be equal to the corresponding Q_{crit} at each temperature point. Interestingly, it can be noticed from Fig. 8 that PW_{Min} in both designs increases with temperature. At high temperature, FinFET designs show better ability to withstand high-energy particle strikes with increasing Q_{crit} or decreasing P_{SET}. The higher strike energy greatly contributes to the extension of PW_{Min} in FinFET circuits. Since the threshold strike energy is very low for planar designs, circuit variation plays a more significant role in defining PW_{Min}. The weaker drive current at higher temperature in conventional designs shows poor resistance to even small amount of charge deposition. For this reason, although Q_{crit} of planar designs decreases as temperature increases, PW_{Min} of the SET current goes wider. This moderate influence of temperature on PW_{Min} as illustrated in Fig. 8 is one of the important factors that contributes to the overall thermal impact on $P_{Latch,min}$.

Setup and hold time window ($t_{S\text{-}H}$) of a flip-flop is another factor of P_{Latch} that depends on temperature. Since $t_{S\text{-}H}$ is essentially the propagation delay of a logic path inside the latch, the change in $t_{S\text{-}H}$ over temperature follows the response of delay to temperature as discussed in Section 2. Fig. 9 shows the plots of $t_{S\text{-}H}$ and temperature for a D flip-flop designed with the same FinFET technology (Fig. 9(a)) and planar MOSFET technology (Fig. 9(b)). As temperature increases, $t_{S\text{-}H}$ of the FinFET flip-flop decreases due to the inversion of temperature effect, whereas $t_{S\text{-}H}$ of the conventional design increases. To see the thermal dependence of $P_{LatchMin}$ of the FinFET and planar inverters operating at a particular frequency, the relationship between the term $PW_{Min} - t_{S-H}$ in (15) and temperature is plotted in Fig. 10. According to (15), if the operating frequency does not change, $P_{LatchMin}$ and $PW_{Min} - t_{S-H}$ are directly proportional. We can imply from Fig. 10 that $P_{LatchMin}$ of both designs increases linearly with temperature. For these two nanoscale technologies, $t_{S\text{-}H}$ is relatively insignificant compared to PW_{Min}. Thus, $P_{LatchMin}$ of both designs strongly relies on PW_{Min}. In addition, frequency and P_{Latch} also have a proportional relationship. We will discuss the impact of frequency variation on soft errors later in Section 4.4.

In conclusion, two of the soft error masking probabilities that are affected by temperature variation in modern designs are P_{SET} and P_{Latch}. The profiles of P_{SET} and $P_{LatchMin}$ under the temperature effect for all library gates can be obtained by extensive device-level SPICE simulation. The simulation results show the exponential decrease of P_{SET} of all gates as a results of the inversion of temperature effect that raises Q_{crit} at high temperature. Additionally, $P_{LatchMin}$ of all gates tends to increase slightly as temperature increases, mainly due to the increase in PW_{Min} with higher strike energy. It is interesting that the temperature effect provides better soft error tolerance for all gates at high temperature. These two temperature-dependent masking probabilities are consequently taken in soft error evaluation for large logic circuits as will be discussed in the following subsections.

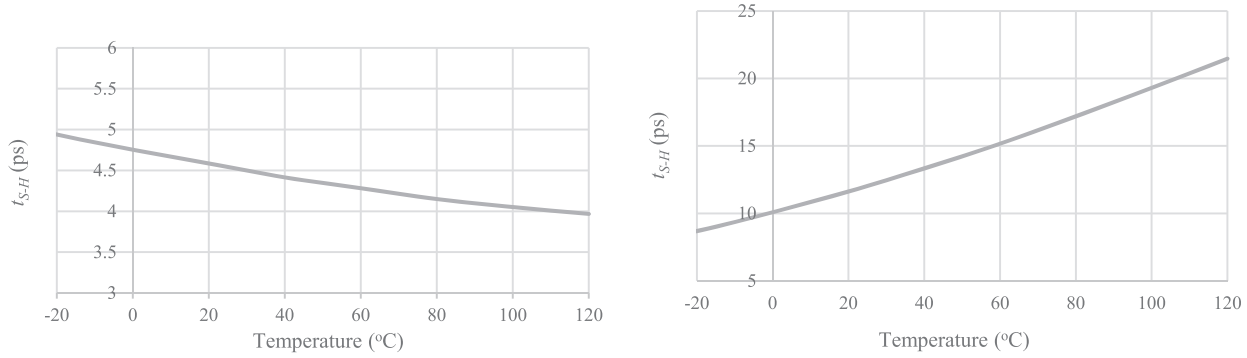
4.3. Impact of supply voltage on SET

Since P_{SET} and P_{Latch} correlate strongly with driving capability of the device, varying supply voltage that has a significant impact on the drive current affects prominently the change in these masking probabilities. The increase in the drive current of FinFETs with increasing supply voltage and rising temperature causes Q_{crit} to increase as evidenced by Fig. 11. Fig. 11 illustrates the relationship between neutron-induced Q_{crit} and supply voltage of the 14-nm FinFET inverter for different temperatures and strike positions. Q_{crit} and supply voltage plots for the strike at the pull-down nFinFET and pull-up pFinFET of the inverter are given in Fig. 11(a) and Fig. 11(b), respectively. We can notice in these figures that the increase in Q_{crit} from increased supply voltage is very large, while the higher temperature provides an additionally moderate



(a) FinFET inverter (b) Planar MOSFET inverter

Fig. 8. PW_{min}vs. temperature in an inverter designed with (a) 14-nm bulk tri-gate FinFET technology and (b) 22-nm high-k/metal gate MOSFET technology.



(a) FinFET technology (b) Planar MOSFET technology

Fig. 9. Setup and hold time window vs. temperature of a D flip-flop for (a) 14-nm bulk tri-gate FinFET technology and (b) 22-nm high-k/metal gate MOSFET technology.

increase in Q_{crit}.

Q_{crit} under temperature and supply voltage variations also varies PW_{min} that is a major factor of $P_{LatchMin}$. Fig. 12(a) and Fig. 12(b) show the plots of $PW_{min} - t_{S\text{-}H}$ and supply voltage of the inverter operating at different temperatures for the strike at the pull-down and pull-up transistors, respectively. At high supply voltage, the term $PW_{min} - t_{S\text{-}H}$ that represents $P_{LatchMin}$ per unit frequency is seen to increase with increasing supply voltage and rising temperature for both strike situations. However, we may see an increase of $P_{LatchMin}$ in some gates/circuits working at near-threshold voltage and low temperature because very weak drive current provides poor pulsewidth suppression. On the other hand, frequency is another important factor that has a directly proportional relationship with $P_{LatchMin}$. If frequency variation is taken into account, the profile of $PW_{min} - t_{S\text{-}H}$ for the gate in Fig. 12 will be scaled by the operating frequency. The overall soft error rate of the circuit is also directly proportional to frequency.

The profiles of Q_{crit} and $PW_{min} - t_{S\text{-}H}$ for all other library gates under supply voltage and temperature variations (similar to Fig. 11 and Fig. 12) can be obtained from device-level simulation.

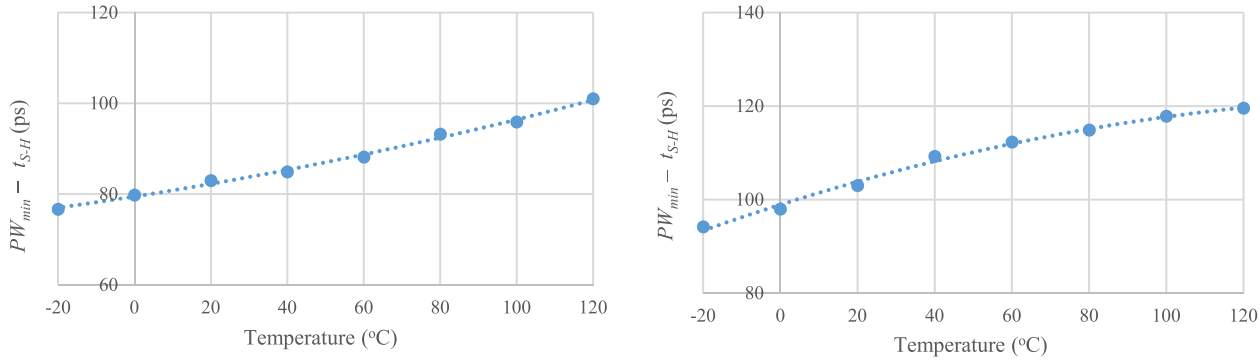
4.4. Temperature dependence of soft errors in logic circuits under supply voltage variation

This part of our work investigates the temperature dependence of soft errors, while supply voltage is varied. To begin with, as SET generation is highly dependent on the circuit input, the proposed soft error simulation adheres strictly to this property. Considering SER for a strike at transistor i or SER_i in (13), SER for any strike inside gate k (SER_k) can be obtained by summing each SER_i corresponding to a strike at transistor i in gate k. To deal with the input dependence of soft errors, we slightly modify (13) by adding the input probability (P_{Input}) to weight the ability to generate SET for different input vectors. The lower bound of SER for a strike inside gate k ($SER_{Min,k}$) can be obtained as follows.

$$SER_{Min,k} = \varphi \bullet P_{Logic,k} \bullet \sum_i \left[A_{active,i,k} \bullet \sum_j \left[P_{Input,j,k} \bullet P_{SET,i,j,k} \bullet P_{LatchMin,i,j,k} \right] \right] \quad (16)$$

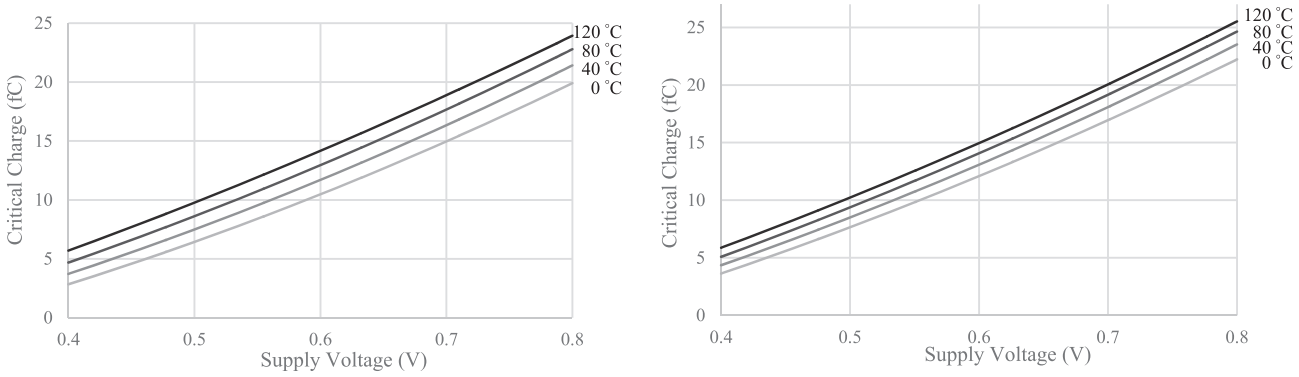
where $P_{Logic,k}$ is the logical masking probability that the SET pulse from gate k can reach the input of a latch element. $P_{Input,j,k}$ is the probability that gate k has an input j. $P_{SET,i,j,k}$ and $P_{LatchMin,i,j,k}$ are the SET generation and minimum latching-window masking probabilities, respectively. Note that $SER_{Min,k}$ is resulted from SER for a strike at each transistor i, for each input j. We assume that the electrical masking probability is always 1 for all strikes. The thermal profiles of Q_{crit}, PW_{Min}, and $t_{S\text{-}H}$ of the library gates and D flip-flop that define $P_{SET,i,j,k}$ and $P_{LatchMin,i,j,k}$ can be exhaustively evaluated by HSPICE with the SET current model in (12). For some parallel devices sharing the same circuit node, the parallel network is considered equivalent to one transistor i with $A_{active,i}$ that covers all drain fins of those parallel devices.

Considering the input dependence of the generation of SET, any transistor in a gate is considered sensitive to the particle strike if the following conditions are satisfied. First, the sensitive device must have already turned off before the strike forces it to turn on and second, path of either parallel or series network to the gate output must be sensitized just after the strike to send the flip to the gate output. Fig. 13 illustrates all possible particle strikes and their equivalent SET current sources injecting into circuit nodes in a 2-input NAND designed with two 1-fin pFinFETs in parallel (P1 and P2) and two 2-fin nFinFETs (N1 and N2) in series. The parallel pull-up network of the 2-input NAND is sensitive to



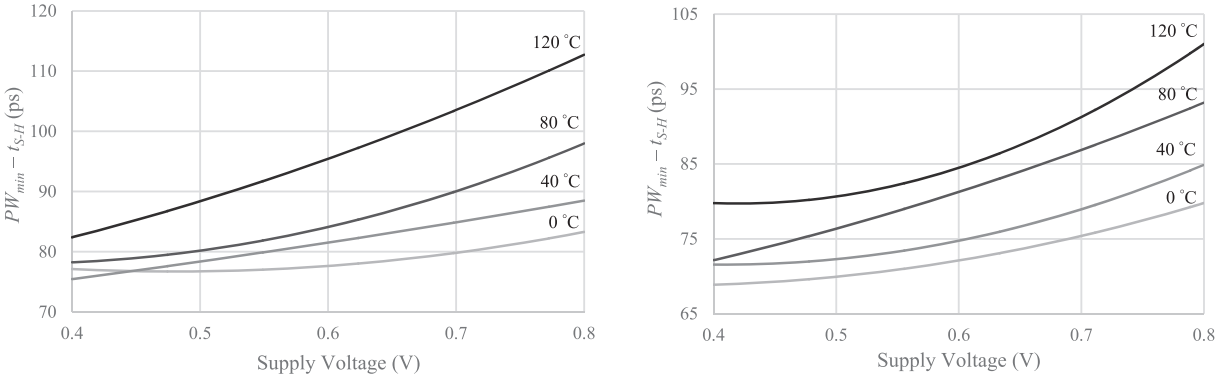
(a) FinFET technology (b) Planar MOSFET technology

Fig. 10. ($PW_{min} - t_{S-H}$) vs. temperature of an inverter with D flip-flop for (a) 14-nm bulk tri-gate FinFET technology and (b) 22-nm high-k/metal gate MOSFET technology.



(a) Strike at the pull-down transistor with input logic "0" (b) Strike at the pull-up transistor with input logic "1"

Fig. 11. Critical charge vs. supply voltage for a neutron strike in an inverter designed with 14-nm bulk tri-gate FinFET technology.



(a) Strike at the pull-down transistor with input logic "0" (b) Strike at the pull-up transistor with input logic "1"

Fig. 12. $PW_{min} - t_{S\text{-}H}$ vs. supply voltage for a neutron strike in an inverter designed with 14-nm bulk tri-gate FinFET technology.

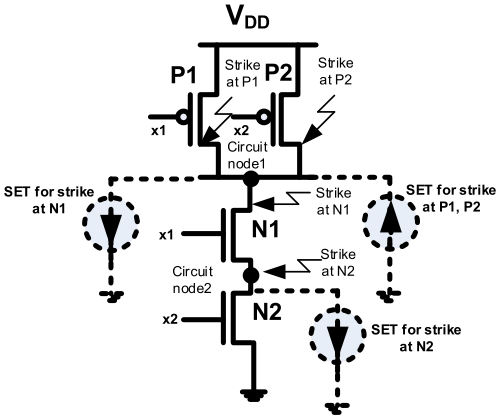


Fig. 13. All possible particle strikes and their equivalent SET current sources injecting into two circuit nodes in a 2-input NAND.

Table 3
Q_{crit} and PW_{min} for a particle strike at each device for all input combinations of a two-input NAND operating at 40 °C.

Input ($x1x2$)	P1, P2		N1		N2	
	Q_{crit} (fC)	PW_{min} (ps)	Q_{crit} (fC)	PW_{min} (ps)	Q_{crit} (fC)	PW_{min} (ps)
00	NS*	NS	NS	NS	NS	NS
01	NS	NS	21.46	93.72	NS	NS
10	NS	NS	NS	NS	21.40	93.90
11	29.50	104.95	NS	NS	NS	NS

* NS = not sensitive.

the particle strike when both P1 and P2 are off ("x1x2" = "11"), and we inject the SET current into circuit node1 to upset each of them. In this situation, the active area for the strike covers the area of two drain fins from P1 and P2. On the other hand, if we inject the SET current into circuit node1 with opposite direction to perform a strike at N1, transistor N2 must have turned on to enable the path to the ground ("x1x2" = "01") and the active area is now the area of two drain fins of N1. In the series network, N2 is considered sensitive when N1 is on ("x1x2" = "10") and we can simulate the strike at N2 by injecting the SET current into circuit node2. For any input vector that turns on all parallel devices (all 0 s for NANDs and all 1 s for NORs), none of the devices is sensitive to the strike, causing very large Q_{crit} or small P_{SET}. Table 3 contains Q_{crit} and PW_{Min} for all transistors in the 2-input NAND in Fig. 13 operating at 40 °C. For most CMOS gates, Q_{crit} of transistors in the series network is generally low compared to Q_{crit} of parallel transistors, but gate input vectors and active area also strongly impact the gate/circuit SER. The overall SER_{Min} of a circuit can be achieved by summing $SER_{Min,k}$ for each gate k in the circuit.

As we focus on addressing soft errors under temperature effect and supply voltage variation, comparative results of $SER_{Min,k}$ with respect to the reference level are considered to simplify the simulation and analysis methodology. This allows us to exclude the particle flux, frequency, and logical masking probability, which are assumed independent of temperature and supply voltage, from soft error evaluation. The normalized $SER_{Min,k}$ ($\widetilde{SER}_{Min,k}$) of gate k operating at a particular temperature T and supply voltage V_{dd} with respect to $SER_{Min,k}$ at the reference temperature T_{ref} and supply voltage V_{ref} is defined as follows.

$$\widetilde{SER}_{Min,k} = \frac{SER_{Min,k}(T, V_{dd})}{SER_{Min,k}(T_{ref}, V_{ref})} = \frac{\sum_i \left[A_{active,i,k} \bullet \sum_j \left[P_{Input,j,k} \bullet P_{SET,i,j,k}(T, V_{dd}) \bullet P_{LatchMin,i,j,k}(T, V_{dd}) \right] \right]}{\sum_i \left[A_{active,i,k} \bullet \sum_j \left[P_{Input,j,k} \bullet P_{SET,i,j,k}(T_{ref,V_{ref}}) \bullet P_{LatchMin,i,j,k}(T_{ref,V_{ref}}) \right] \right]} \quad (17)$$

A key metric we use to evaluate thermal response of soft errors in the experimental circuits is the average of $\widetilde{SER}_{Min,k}$ of all gates in the circuit. This average of the normalized minimum gate SER of a circuit denoted as $\langle \widetilde{SER}_{GateMin} \rangle$ is given below.

$$\langle \widetilde{SER}_{GateMin} \rangle = \frac{\widetilde{SER}_{Min,k}}{total\ number\ of\ gates} \quad (18)$$

We evaluate $\langle \widetilde{SER}_{GateMin} \rangle$ for each selected circuit from ISCAS-85/89 and MCNC benchmark suites. All experimental circuits are designed with 14-nm bulk tri-gate FinFET predictive technology from [33]. Our cell library for technology mapping includes the inverter, 2-, 3-, and 4-input NAND/NOR gates, and D flip-flop. Each primary output of the logic circuit is connected to a flip-flop. P_{Input} for each gate is obtained from logic simulation with the equally weighted logic applied to each primary input of the circuit, and other related device-level parameters (e.g., Q_{crit}, PW_{min}, and $t_{S\text{-}H}$) are identified using HSPICE. All circuits are assessed under supply voltage and temperature variations with $LET = 50$ nC/μm, and $L_c = 50$ nm.

Table 4 contains $\langle \widetilde{SER}_{GateMin} \rangle$ of the experimental logic circuits operating at different supply voltages of 0.4 V, 0.6 V, and 0.8 V and temperatures of 0 °C, 40 °C, 80 °C, and 120 °C. The reference temperature and supply voltage for this simulation are set to $T_{ref} = 0$ °C and $V_{ref} = 0.4$ V, respectively. As supply voltage increases, we can see that all $\langle \widetilde{SER}_{GateMin} \rangle$ results drop dramatically. On average, $\langle \widetilde{SER}_{GateMin} \rangle$ results at 0 °C for the supply voltages of 0.6 V and 0.8 V fall from the reference level (100% at 0 °C and 0.4 V) to as low as 3.7% and 0.08%, respectively. Furthermore, the increase in temperature additionally provides a moderate reduction in soft errors for all circuits. When temperature increases from 0 °C to 40 °C, 80 °C, and 120 °C, the circuits with the same level of supply voltage experience further decrease in $\langle \widetilde{SER}_{GateMin} \rangle$ down to roughly 70%, 50%, and 30% of the average result at 0 °C, respectively. The decrease in soft error rate with increasing supply voltage and temperature as reported in Table 4 is mainly influenced by the decrease of P_{SET}. As evident by Fig. 6 in Section 4.2 and Fig. 11 in Section 4.3, the impact of supply voltage is found to be strong compared to the temperature effect providing a large rise in Q_{crit} and a sharp drop in P_{SET}. Because the impacts of supply voltage and temperature on $P_{LatchMin}$ are small, soft error immunity is strongly dependent on the change of P_{SET}. In addition, frequency is one of the key circuit parameters that greatly affect soft errors. Due to the fact that frequency and soft error rate have a directly proportional relationship, if we consider the change in operating frequency (f) from the reference level (f_{ref}), all results in Table 4 will be scaled by the factor of f/f_{ref}.

While some major reliability-related mechanisms, such as electromigration, oxide breakdown, and device variability degradation are worsened by increased temperature, our investigation raises awareness about soft error reliability that improves at high temperature. Due to heat issues in 3-D technology, promising thermal management techniques are mandatory to control the chip temperature in most processors. It is suggested that the importance of temperature optimization be considered well in future designs where the thermal responses of key performance- and reliability-related mechanisms are somewhat diverse. This investigation provides a potential future direction of improving thermal management considering the impact of temperature and supply voltage on BTI and soft errors. The correlations of electrical power and temperature highly rely on heat dissipation to the ambience which is characterized by material, dimension, and ambient temperature of the die. In addition, the MOL and BEOL also play important roles in thermal performance and reliability of the chip. In this study, all die temperatures were set independently regardless of considering the aforementioned heat transfer parameters. However, whenever those thermal factors are fully achieved, the die temperature can be derived earlier from power/thermal characteristics of the chip. The proposed methodology for evaluating thermal impacts on BTI and soft errors under circuit parameter variations can well be used for any arbitrary temperature.

5. Conclusion

This study investigates the impact of temperature on BTI and soft errors in modern digital circuits. The inversion of temperature effect, which strengthens the drive current of FinFET designs at high temperature, is found to have a significant influence on circuit performance. We model the temperature effect as a source of threshold voltage variation which is consequently taken in simulation and analysis of BTI degradation in large logic circuits. Under 10-year BTI stress, the delay results of the experimental circuits (in Table 2) from the proposed estimation where the temperature effect is considered are slightly more pessimistic than that from the conventional approach. Although the results of BTI aging delay of all circuits worsen at high temperature, the domination of temperature-induced performance improvement to BTI degradation causes all experimental circuits to run faster at higher operating temperature. We also evaluate the impact of temperature and supply voltage on logic soft errors. The results in Table 4 show that soft error rate drops significantly as supply voltage and temperature increase. The decrease in soft error rate is mainly influenced by the increase of critical charge. On average, the results of the relative soft error rate at 0 °C for the supply voltages of 0.6 V and 0.8 V decrease to as low as 3.7% and 0.08% of the average result at 0.4 V, respectively. When

Table 4
The average of the normalized minimum gate SER under supply voltage and temperature variations with $T_{ref} = 0$ °C and $V_{ref} = 0.4$ V.

Circuit	$\langle \widetilde{SER}_{GateMin} \rangle \times 100$											
	$V_{dd} = 0.4$ V				$V_{dd} = 0.6$ V				$V_{dd} = 0.8$ V			
	0 °C	40 °C	80 °C	120 °C	0 °C	40 °C	80 °C	120 °C	0 °C	40 °C	80 °C	120 °C
C1908	100	71.66	51.67	37.93	3.756	2.451	1.649	1.186	0.0815	0.0492	0.0327	0.0243
C6288		72.60	52.59	39.58	3.130	2.122	1.488	1.118	0.0558	0.0356	0.0252	0.0201
C7552		71.91	51.85	38.32	3.983	2.607	1.746	1.244	0.0890	0.0534	0.0352	0.0259
i7		71.25	51.02	37.47	3.634	2.374	1.603	1.148	0.0775	0.0468	0.0312	0.0232
i8		71.36	51.40	37.68	3.524	2.301	1.561	1.128	0.0740	0.0450	0.0300	0.0224
i9		71.54	51.55	38.01	3.528	2.324	1.579	1.143	0.0728	0.0445	0.0299	0.0225
S5378		72.92	53.23	40.08	3.854	2.579	1.742	1.261	0.0823	0.0499	0.0335	0.0252
S15850		72.34	52.40	39.01	4.080	2.688	1.798	1.282	0.0913	0.0548	0.0362	0.0267
S35932		71.66	51.65	37.88	3.995	2.598	1.734	1.236	0.0898	0.0539	0.0355	0.0260
Average	100	71.92	51.93	38.44	3.720	2.449	1.656	1.194	0.0793	0.0481	0.0322	0.0240

temperature varies from 0 °C to 40 °C, 80 °C, and 120 °C, the circuits experience further decrease in the relative soft error rate down to roughly 70%, 50%, and 30% of the average result at 0 °C, respectively.

Acknowledgement

This work was supported in part by Rajamangala University of Technology Phra Nakhon under Project 60210601, and the National Science and Technology Development Agency under Project SCH-NR2014-271.

References

[1] S.E. Liu, J.S. Wang, Y.R. Lu, D.S. Huang, C.F. Huang, W.H. Hsieh, J.H. Lee, Y.S. Tsai, J.R. Shih, Y.H. Lee, K. Wu, Self-heating effect in FinFETs and its impact on devices reliability characterization, IEEE Int. Reliab. Phys. Symp., Waikoloa, HI, USA, 2014, http://dx.doi.org/10.1109/IRPS.2014.6860642.

[2] C. Xu, S.K. Kolluri, K. Endo, K. Banerjee, Analytical thermal model for self-heating in advanced FinFET devices with implications for design and reliability, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 32 (2013) 1045–1058, http://dx.doi.org/10.1109/TCAD.2013.2248194.

[3] C. Prasad, L. Jiang, D. Singh, M. Agostinelli, C. Auth, P. Bai, T. Eiles, J. Hicks, C.H. Jan, K. Mistry, S. Natarajan, B. Niu, P. Packan, D. Pantuso, I. Post, S. Ramey, A. Schmitz, B. Sell, S. Suthram, J. Thomas, C. Tsai, P. Vandervoorn, Self-heat reliability considerations on Intel's 22 nm Tri-Gate technology, IEEE Int. Reliab. Phys. Symp., Anaheim, CA, USA, 2013, http://dx.doi.org/10.1109/IRPS.2013.6532036.

[4] M.C. Cheng, J.A. Smith, W. Jia, R. Coleman, An effective thermal model for FinFET structure, IEEE Trans. Electron Devices 61 (2014) 202–206, http://dx.doi.org/10.1109/TED.2013.2291512.

[5] U.S. Kumar, V.R. Rao, A thermal-aware device design considerations for nanoscale SOI and bulk FinFETs, IEEE Trans. Electron Devices 63 (2016) 280–287, http://dx.doi.org/10.1109/TED.2015.2502062.

[6] A.L. Zimpeck, C. Meinhardt, R.A.L. Reis, Impact of PVT variability on 20 nm FinFET standard cells, Microelectron. Reliab. 55 (2015) 1379–1383, http://dx.doi.org/10.1016/j.microrel.2015.06.039.

[7] W. Lee, Y. Wang, T. Cui, S. Nazarian, M. Pedram, Dynamic thermal management for FinFET-based circuits exploiting the temperature effect inversion phenomenon, Proc. Int. Symp. Low Power Electron. Des., La Jolla, CA, USA, 2014, pp. 105–110, , http://dx.doi.org/10.1145/2627369.2627608.

[8] S. Khan, I. Agbo, S. Hamdioui, H. Kukner, B. Kaczer, P. Raghavan, F. Catthoor, Bias temperature instability analysis of FinFET based SRAM cells, Des. Autom. Test Eur. Conf. Exhib., Dresden, Germany, 2014, pp. 1–6, , http://dx.doi.org/10.7873/DATE.2014.044.

[9] W. Sootkaneung, S. Howimanporn, S. Chookaew, Thermal effect on performance, power, and BTI aging in FinFET-based designs, Proc. Euromicro Conf. Digit. Syst. Des., Vienna, Austria, 2017, pp. 345–351, , http://dx.doi.org/10.1109/DSD.2017.35.

[10] Y. Zhang, S.S. Chen, L. Peng, S.S. Chen, Mitigating NBTI degradation on FinFET GPUs through exploiting device heterogeneity, IEEE Comput. Soc. Annu. Symp. VLSI, Tempa, FL, USA, 2014, pp. 577–582, , http://dx.doi.org/10.1109/ISVLSI.2014.21.

[11] H. Kukner, M. Khatib, S. Morrison, P. Weckx, P. Raghavan, B. Kaczer, F. Catthoor, L. Van Der Perre, R. Lauwereins, G. Groeseneken, Degradation analysis of datapath logic subblocks under NBTI aging in FinFET technology, Int. Symp. Qual. Electron. Des., Santa Clara, CA, USA, 2014, pp. 473–479, , http://dx.doi.org/10.1109/ISQED.2014.6783362.

[12] A. Vijayan, A. Koneru, S. Kiamehr, K. Chakrabarty, M.B. Tahoori, Fine-grained aging-induced delay prediction based on the monitoring of run-time stress, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 37 (2018) 1064–1075 https://doi.org/10.1109/TCAD.2016.2620903.

[13] Y.C. Huang, M.H. Hsieh, T.Y. Yew, W. Wang, D. Maji, Y.H. Lee, W.S. Chou, P.Z. Kang, Delay effects and frequency dependence of NBTI with sub-microsecond measurements, IEEE Int. Reliab. Phys. Symp., Monterey, CA, USA, 2015 (p. 4A21–4A25), https://doi.org/10.1109/IRPS.2015.7112724.

[14] M. Anglada, R. Canal, J.L. Aragón, A. González, MASkIt: soft error rate estimation for combinational circuits, Proc. IEEE Int. Conf. Comput. Des. 2016, pp. 614–621, , http://dx.doi.org/10.1109/ICCD.2016.7753348.

[15] F.S. Alghareb, R.A. Ashraf, A. Alzahrani, R.F. DeMara, Energy and delay tradeoffs of soft-error masking for 16-nm FinFET logic paths: survey and impact of process variation in the near-threshold region, IEEE Trans. Circuits Syst. Express Briefs 64 (2017) 695–699, http://dx.doi.org/10.1109/TCSII.2016.2587763.

[16] J. Li, J. Draper, Joint soft-error-rate (SER) estimation for combinational logic and sequential elements, Proc. IEEE Comput. Soc. Annu. Symp. VLSI, 2016, pp. 737–742, , http://dx.doi.org/10.1109/ISVLSI.2016.28.

[17] L. Artola, M. Gaillardin, G. Hubert, M. Raine, P. Paillet, Modeling single event transients in advanced devices and ICs, IEEE Trans. Nucl. Sci. 62 (2015) 1528–1539, http://dx.doi.org/10.1109/TNS.2015.2432271.

[18] N. Seifert, S. Jahinuzzaman, J. Velamala, R. Ascazubi, N. Patel, B. Gill, J. Basile, J. Hicks, Soft error rate improvements in 14-nm technology featuring second-generation 3D tri-gate transistors, IEEE Trans. Nucl. Sci. 62 (2015) 2570–2577, http://dx.doi.org/10.1109/TNS.2015.2495130.

[19] S. Lee, I. Kim, S. Ha, C.S. Yu, J. Noh, S. Pae, J. Park, Radiation-induced soft error rate analyses for 14 nm FinFET SRAM devices, Proc. IEEE Int. Reliab. Phys. Symp., Monterey, CA, USA, 2015 (p. 4B11–4B14), https://doi.org/10.1109/IRPS.2015.7112728.

[20] H. Liu, M. Cotter, S. Datta, V. Narayanan, Soft-error performance evaluation on emerging low power devices, IEEE Trans. Device Mater. Reliab. 14 (2014) 732–741, http://dx.doi.org/10.1109/TDMR.2014.2316505.

[21] B. Narasimham, S. Hatami, A. Anvar, D.M. Harris, A. Lin, J.K. Wang, I. Chatterjee, K. Ni, B.L. Bhuva, R.D. Schrimpf, R.A. Reed, M.W. McCurdy, Bias dependence of single-event upsets in 16 nm FinFET D-flip-flops, IEEE Trans. Nucl. Sci. 62 (2015) 2578–2584, http://dx.doi.org/10.1109/TNS.2015.2498927.

[22] P. Royer, F. Garcia-Redondo, M. Lopez-Vallejo, Evolution of radiation-induced soft errors in FinFET SRAMs under process variations beyond 22 nm, Proc. IEEE/ACM Int. Symp. Nanoscale Archit., Boston, USA, 2015, pp. 112–117, , http://dx.doi.org/10.1109/NANOARCH.2015.7180596.

[23] S. Kiamehr, T. Osiecki, M. Tahoori, S. Nassif, Radiation-induced soft error analysis of SRAMs in SOI FinFET technology: a device to circuit approach, Proc. Des. Autom. Conf., San Francisco, CA, USA, 2014, pp. 1–6, , http://dx.doi.org/10.1145/2593069.2593196.

[24] N.N. Mahatme, N.J. Gaspard, S. Jagannathan, T.D. Loveless, B.L. Bhuva, W.H. Robinson, L.W. Massengill, S.-J. Wen, R. Wong, Impact of supply voltage and frequency on the soft error rate of logic circuits, IEEE Trans. Nucl. Sci. 60 (2013) 4200–4206, http://dx.doi.org/10.1109/TNS.2013.2288782.

[25] D. Rossi, M. Omaña, C. Metra, A. Paccagnella, Impact of bias temperature instability on soft error susceptibility, IEEE Trans. Very Large Scale Integr. VLSI Syst. 23 (2015) 743–751, http://dx.doi.org/10.1109/TVLSI.2014.2320307.

[26] L. Li, L. Xiao, X. Cao, C. Qi, Z. Mao, Impact of BTI aging effect on soft error rate of combination circuit, Progn. Syst. Heal. Manag. Conf, 2017, pp. 1–5, , http://dx.doi.org/10.1109/PHM.2017.8079142.

[27] W. Sootkaneung, S. Chookaew, S. Howimanporn, Combined impact of BTI and temperature effect inversion on circuit performance, Asian Test Symp., Hiroshima, Japan, 2016, pp. 310–315, , http://dx.doi.org/10.1109/ATS.2016.34.

[28] S. Soleimani, A. Afzali-Kusha, B. Forouzandeh, Temperature dependence of propagation delay characteristic in FinFET circuits, Int. Conf. Microelectron., Sharjah, UAE, 2008, pp. 276–279, , http://dx.doi.org/10.1109/ICM.2008.5393513.

[29] S.-Y. Kim, Y.M. Kim, K.-H. Baek, B.-K. Choi, K.-R. Han, K.-H. Park, J.-H. Lee, Temperature dependence of substrate and drain-currents in bulk FinFETs, IEEE Trans. Electron Devices 54 (2007) 1259–1264, http://dx.doi.org/10.1109/TED.2007.894605.

[30] H. Luo, Y. Wang, K. He, R. Luo, H. Yang, Y. Xie, A novel gate-level NBTI delay degradation model with stacking effect, Int. Conf. Integr. Circuit Syst. Des. Power Timing Model. Optim. Simul., Gothenburg, Sweden, 2007, pp. 160–170, , http://dx.doi.org/10.1007/978-3-540-74442-9.

[31] B.C. Paul, K. Kang, H. Kufluoglu, M.A. Alam, K. Roy, Negative bias temperature instability: estimation and design for improved reliability of nanoscale circuits, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 26 (2007) 743–751, http://dx.doi.org/10.1109/TCAD.2006.884870.

[32] W. Sootkaneung, P. Lapamonpinyo, S. Chookaew, S. Howimanporn, NBTI in FinFET circuits under the temperature effect inversion, IEEE Int. Conf. Comput. Sci. Eng., Paris, France, 2016, pp. 343–350, , http://dx.doi.org/10.1109/CSE-EUC-DCABES.2016.206.

[33] ASU, Predictive technology models, http://www.eas.asu.edu/~ptm, (2012).

[34] M. Cho, J.-D. Lee, M. Aoulaiche, B. Kaczer, P. Roussel, T. Kauerauf, R. Degraeve, J. Franco, L.-Å. Ragnarsson, G. Groeseneken, Insight into N/PBTI mechanisms in sub-1-nm-EOT devices, IEEE Trans. Electron Devices 59 (2012) 2042–2048, http://dx.doi.org/10.1109/TED.2012.2199496.

[35] W. Wang, S. Yang, S. Bhardwaj, S. Vrudhula, F. Liu, Y. Cao, The impact of NBTI effect on combinational circuit: modeling, simulation, and analysis, IEEE Trans. Very Large Scale Integr. VLSI Syst. 18 (2010) 173–183, http://dx.doi.org/10.1109/TVLSI.2008.2008810.

[36] M. Omaña, D. Rossi, T. Edara, C. Metra, Impact of aging phenomena on latches' robustness, IEEE Trans. Nanotechnol. 15 (2016) 129–136, http://dx.doi.org/10.1109/TNANO.2015.2494612.

[37] A. Bansal, M. Meterelliyoz, S. Singh, J.H. Choi, J. Murthy, K. Roy, Compact thermal models for estimation of temperature-dependent power/performance in FinFET technology, Asia South Pacific Conf. Des. Autom., Yokohama, Japan, 2006, pp. 237–242, , http://dx.doi.org/10.1109/ASPDAC.2006.1594688.

[38] V.B. Kleeberger, H. Graeb, U. Schlichtmann, Predicting future product performance: modeling and evaluation of standard cells in FinFET technologies, Des. Autom. Conf., Austin, TX, USA, 2013, pp. 1–6, , http://dx.doi.org/10.1145/2463209.2488775.

[39] D.G. Mavis, P.H. Eaton, Soft error rate mitigation techniques for modern microcircuits, Proc. Reliab. Phys. Symp., Dallas, TX, USA, 2002, pp. 216–225, , http://dx.doi.org/10.1109/RELPHY.2002.996639.

[40] M. Bagatin, S. Gerardin, A. Paccagnella, C. Andreani, G. Gorini, C.D. Frost, Temperature dependence of neutron-induced soft errors in SRAMs, Microelectron. Reliab. 52 (2012) 289–293, http://dx.doi.org/10.1016/j.microrel.2011.08.011.